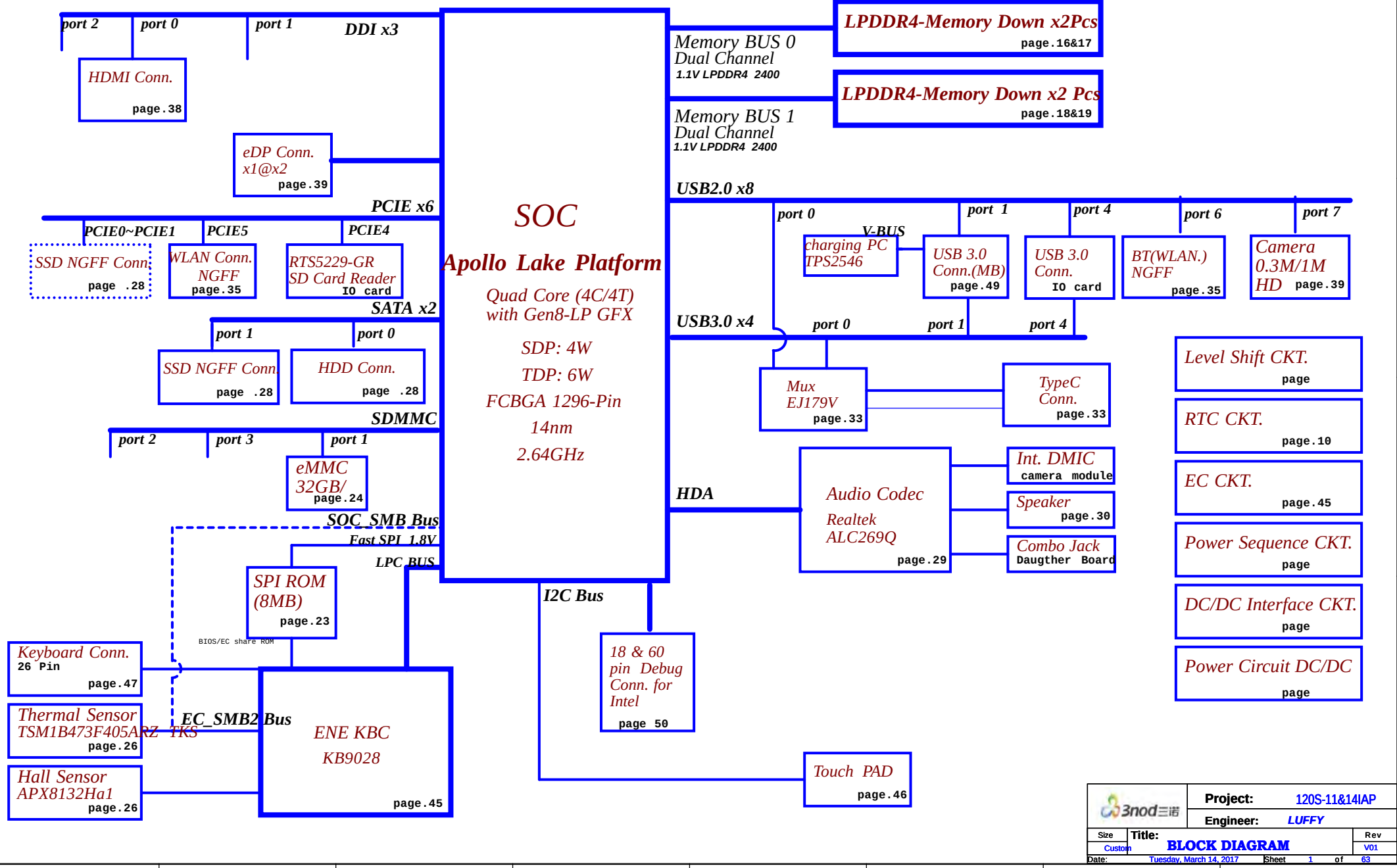
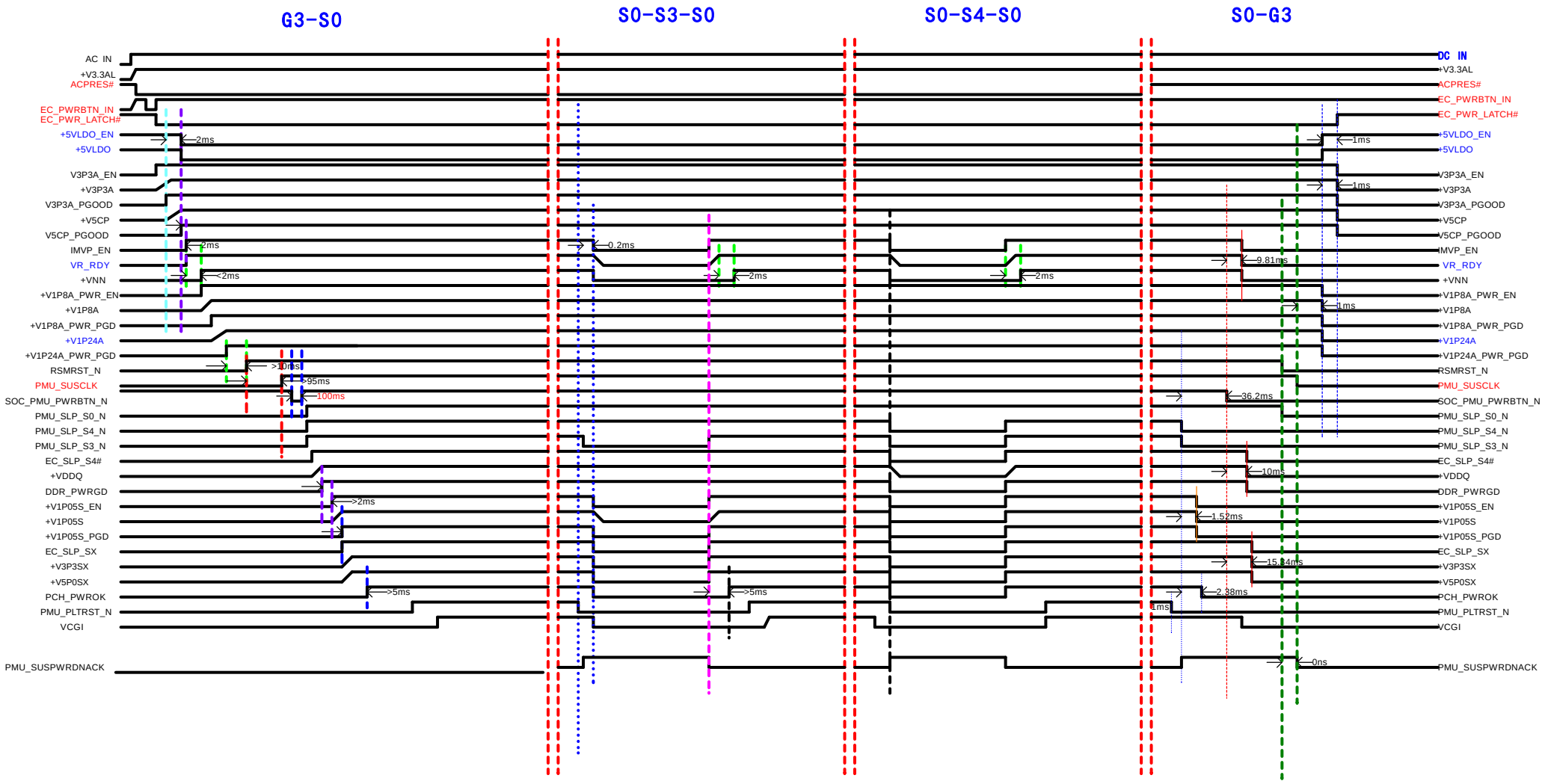
APL MRD FAB A



3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: BLOCK DIAGRAM	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 1 of 63	



INTERNAL ONLY

BPAGE DRAWING

apl_ff.8A
Fri May 27 06:47:24 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: Lear	
Size: Custom	Title: <POWER SEQUENCE>	Rev: V01
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7	APL SOC-PCIE&USB
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9	APL SOC- I2C&HDA
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29	AUDIO CODEC
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31	GAUGE&BATTERY CONN
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34	NC
35	WIFI/BT M.2 CONN
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38	HDMI CONN
39	DISPLAY
40	+V5P0A ,+V3P3SX,+V5P0SX

SHEET NO.	SHEET NAME
41	NC
42	NC
43	NC
44	NC
45	EC-1
46	EC-2 (LED, BUTTON)
47	EC-3 (KEYBOARD,TP CONN)
48	NC
49	USB CHANGER,USB3.0 CONN
50	IO&DEBUG CONN
51	MISC
52	NC
53	SCREW
54	BATTERY CHARGER
55	PWR +V3P3A AND +5CP
56	PWR-DDR
57	PWR-NC
58	PWR-+V1P05S
59	PWR-+V1P24A
60	PWR-+V1P8A
61	VCGI AND VNN_1
62	VCGI AND VNN_2
63	PWR BLOCK DIAGRAM

BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:10 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: TABLE OF CONTENTS	Rev: V01
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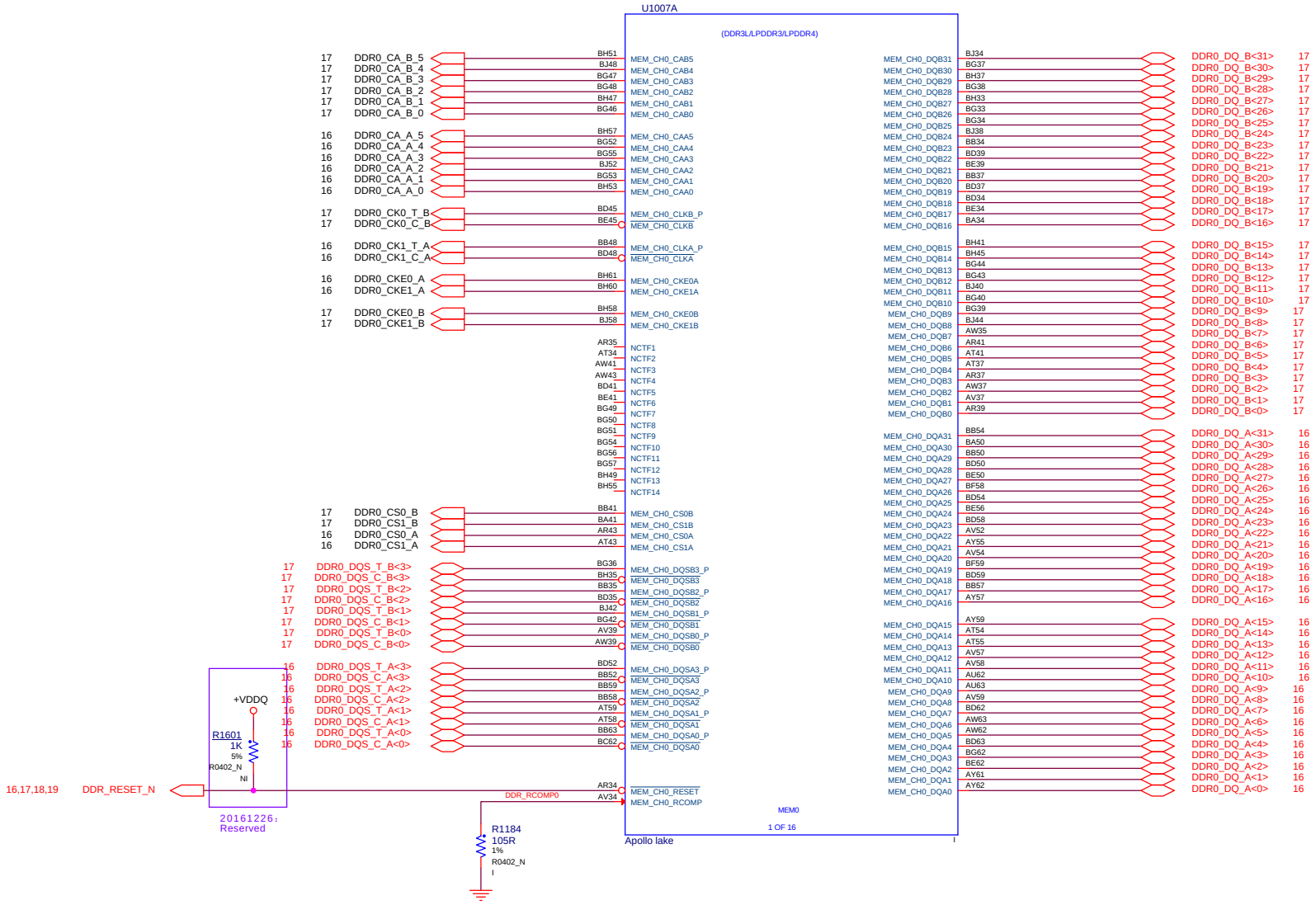

INTERNAL ONLY

BPAGE DRAWING

apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<APL SOC-LPDDR4 CH0>
		Rev: V01
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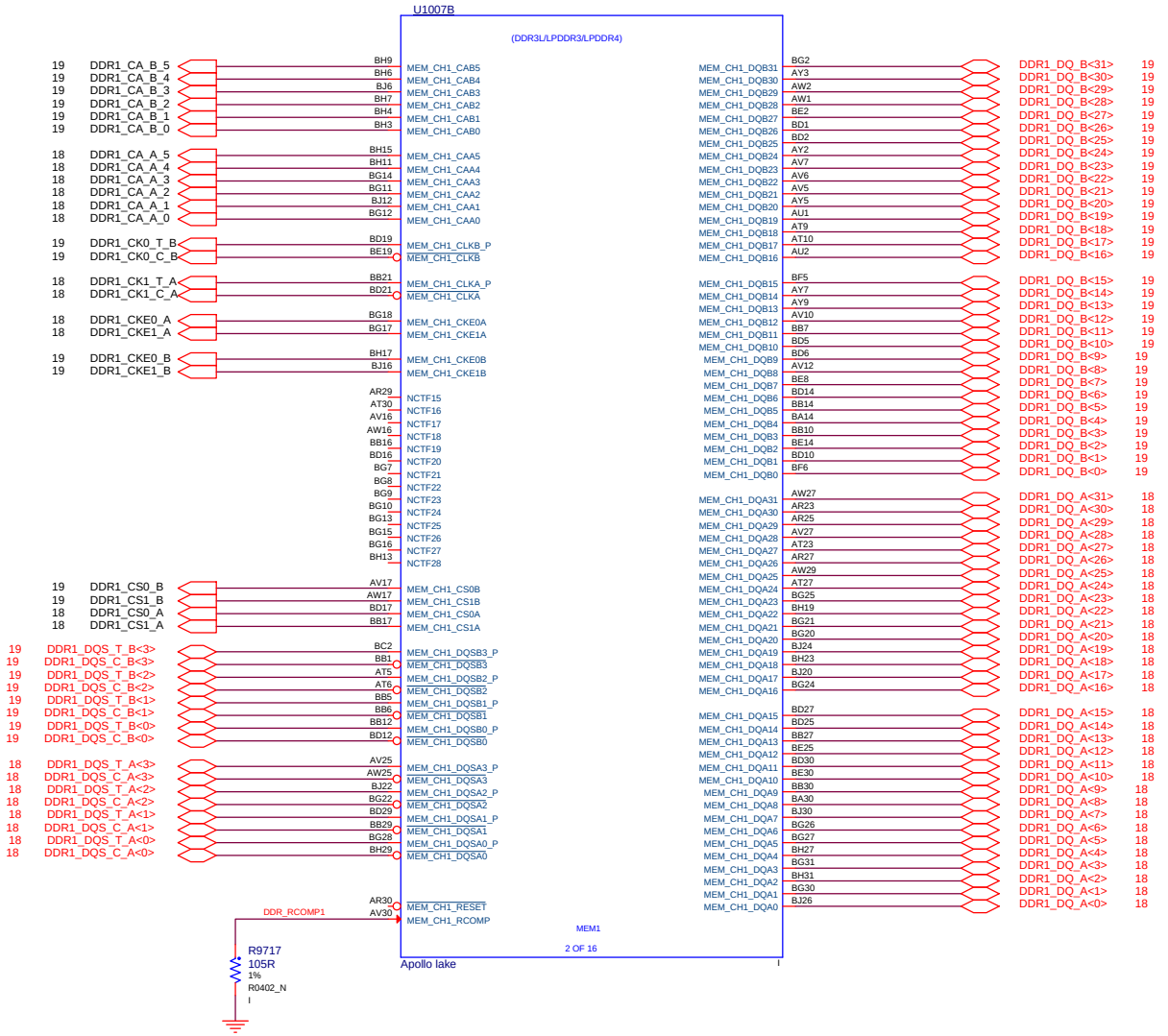
SOC: LPDDR4 CH1



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3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC-LDDR4 CH1	Rev: V01
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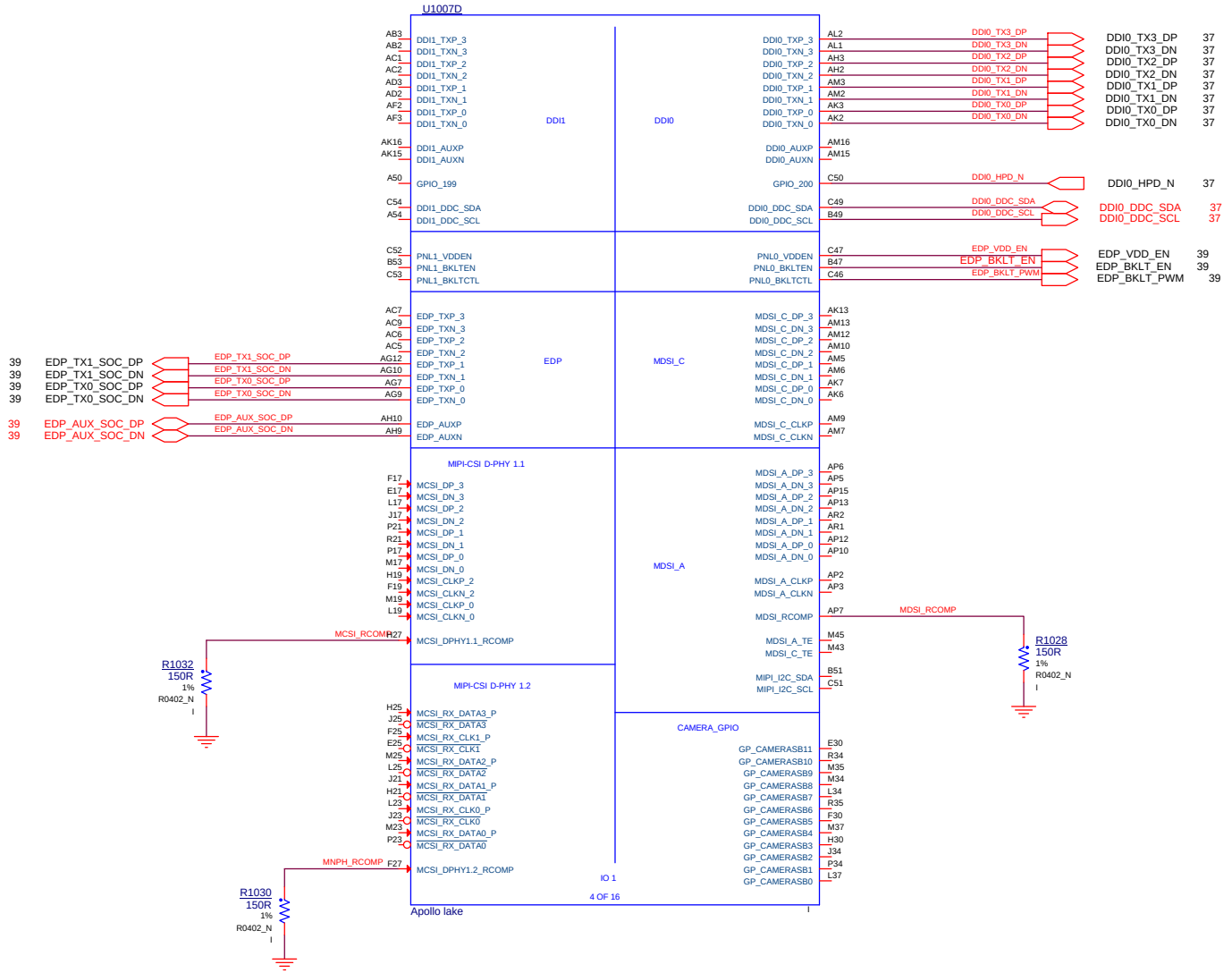

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apl_ff.GND
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3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC-DISPLAY	Rev: V01
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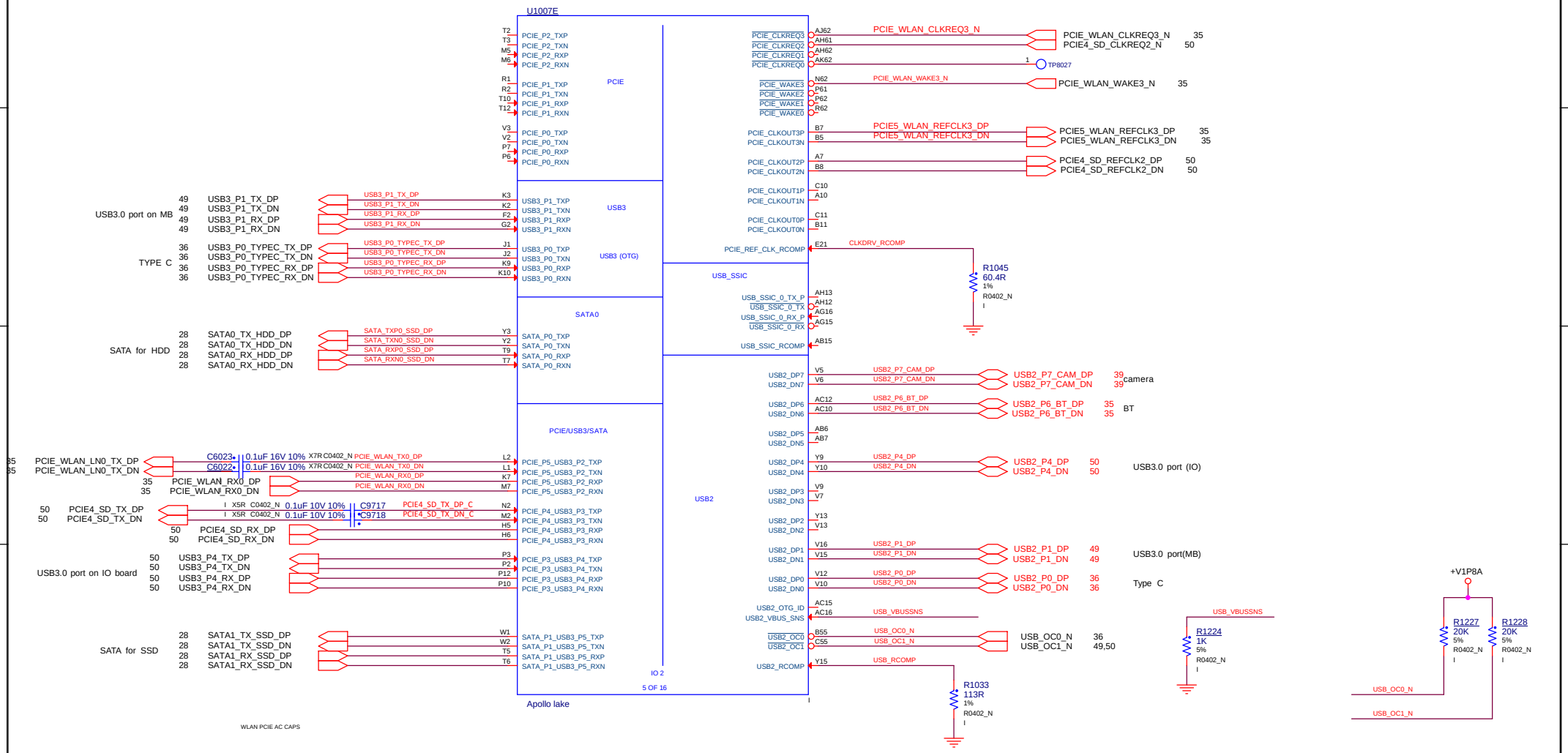

BPAGE DRAWING

apl_ifl.8A

Fri May 27 06:47:12 2016

Project:	120S-11&14IAP	
Engineer:	LUFFY	
Size: Custom	Title: SOC-PCIE&USB	Rev: V01
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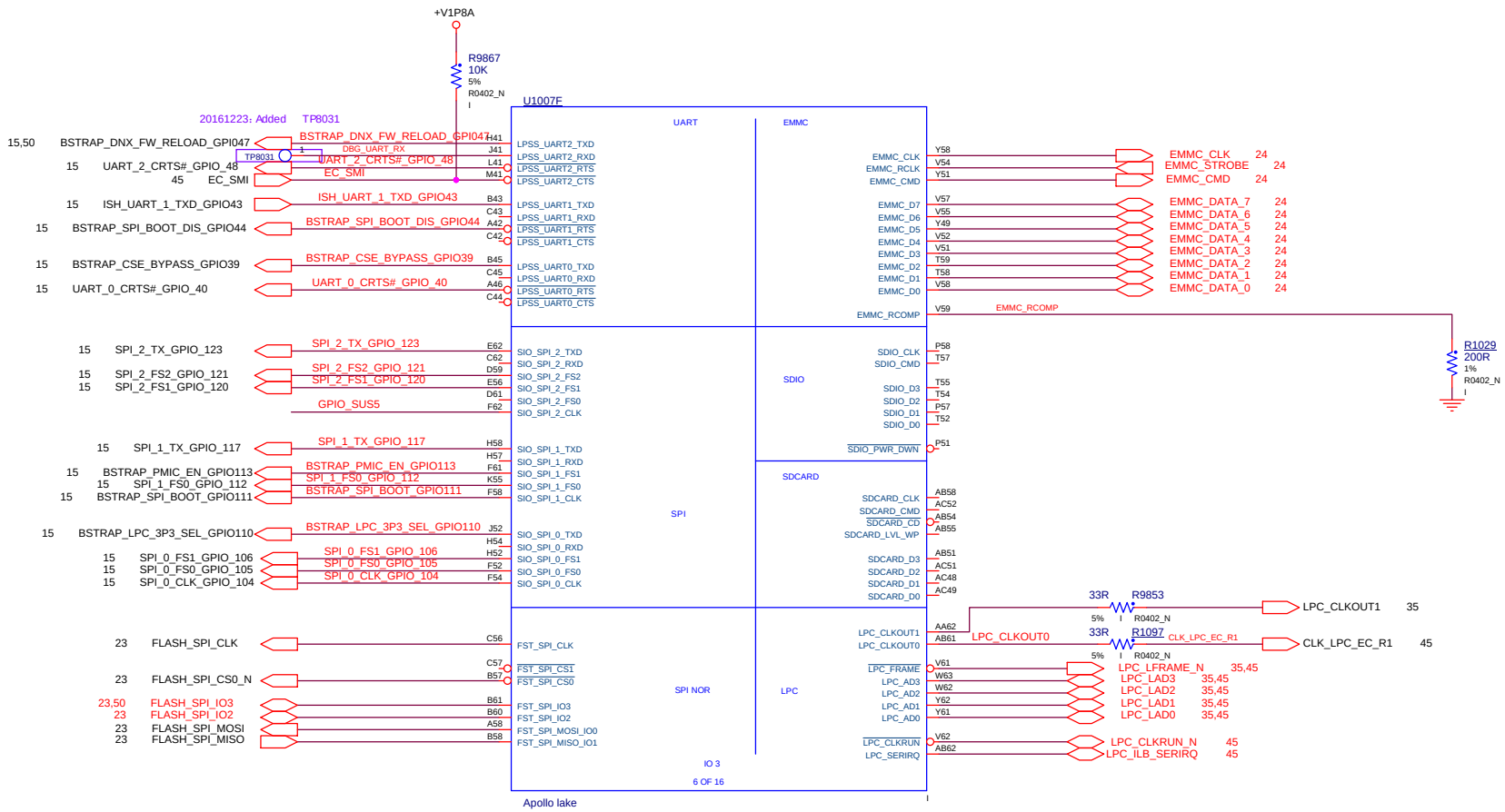
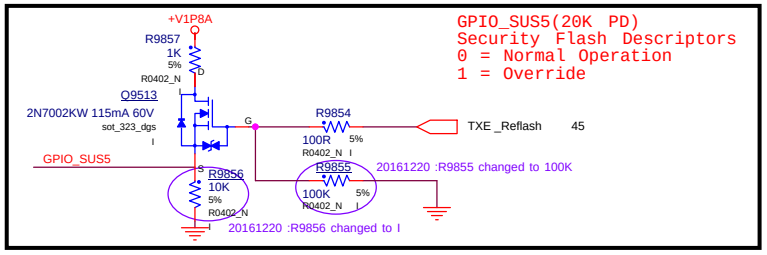
20160712: Change to NI





20161220 :Modified

CONN TBD

R1199 - EMMC BOOT STRAP

BPAGE DRAWING

apl_lf.GND
Fri May 27 06:47:12 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	SOC-EMMC,SPI,LPC
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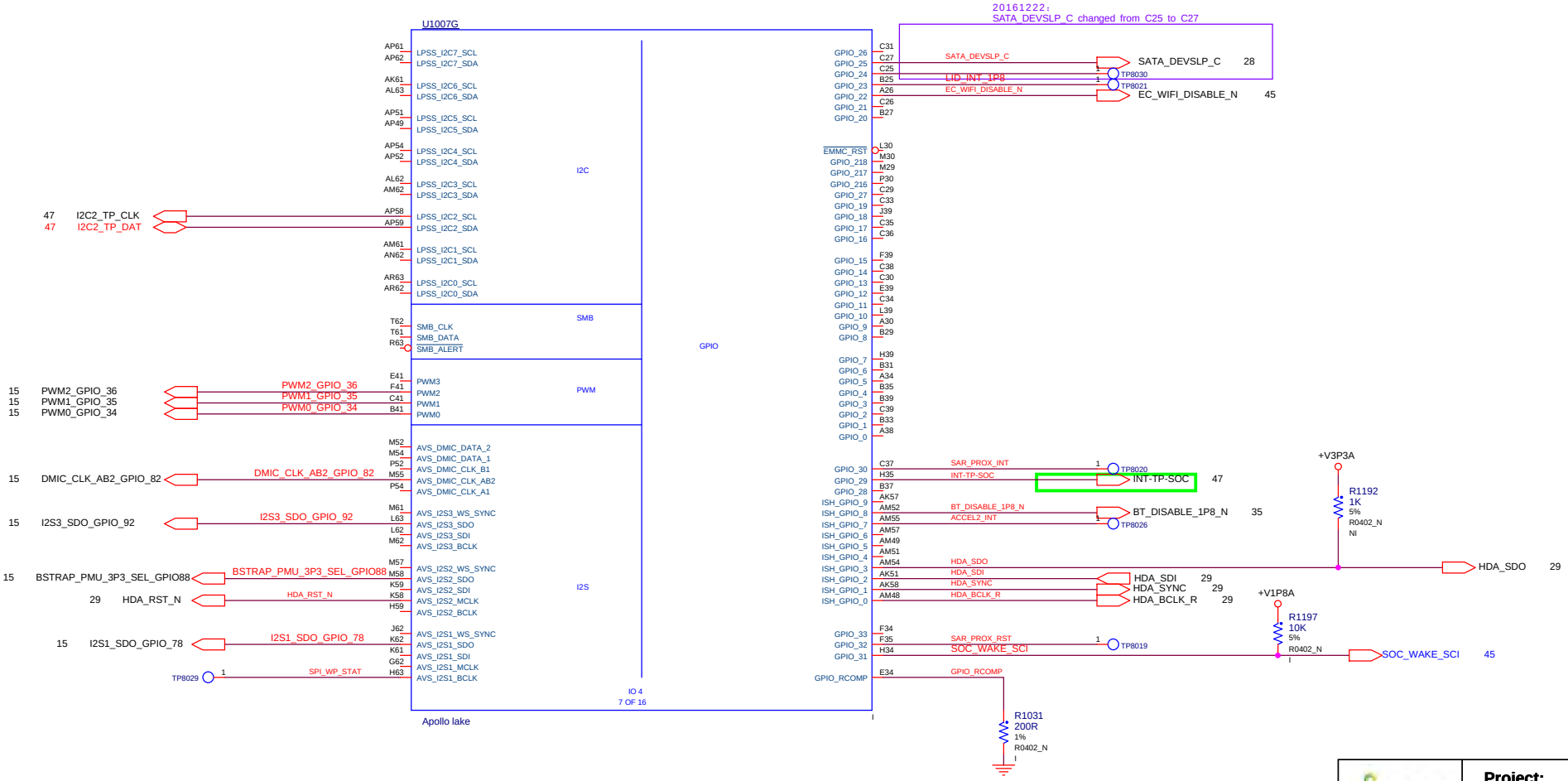

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3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC- I2C&HDA	Rev: V01
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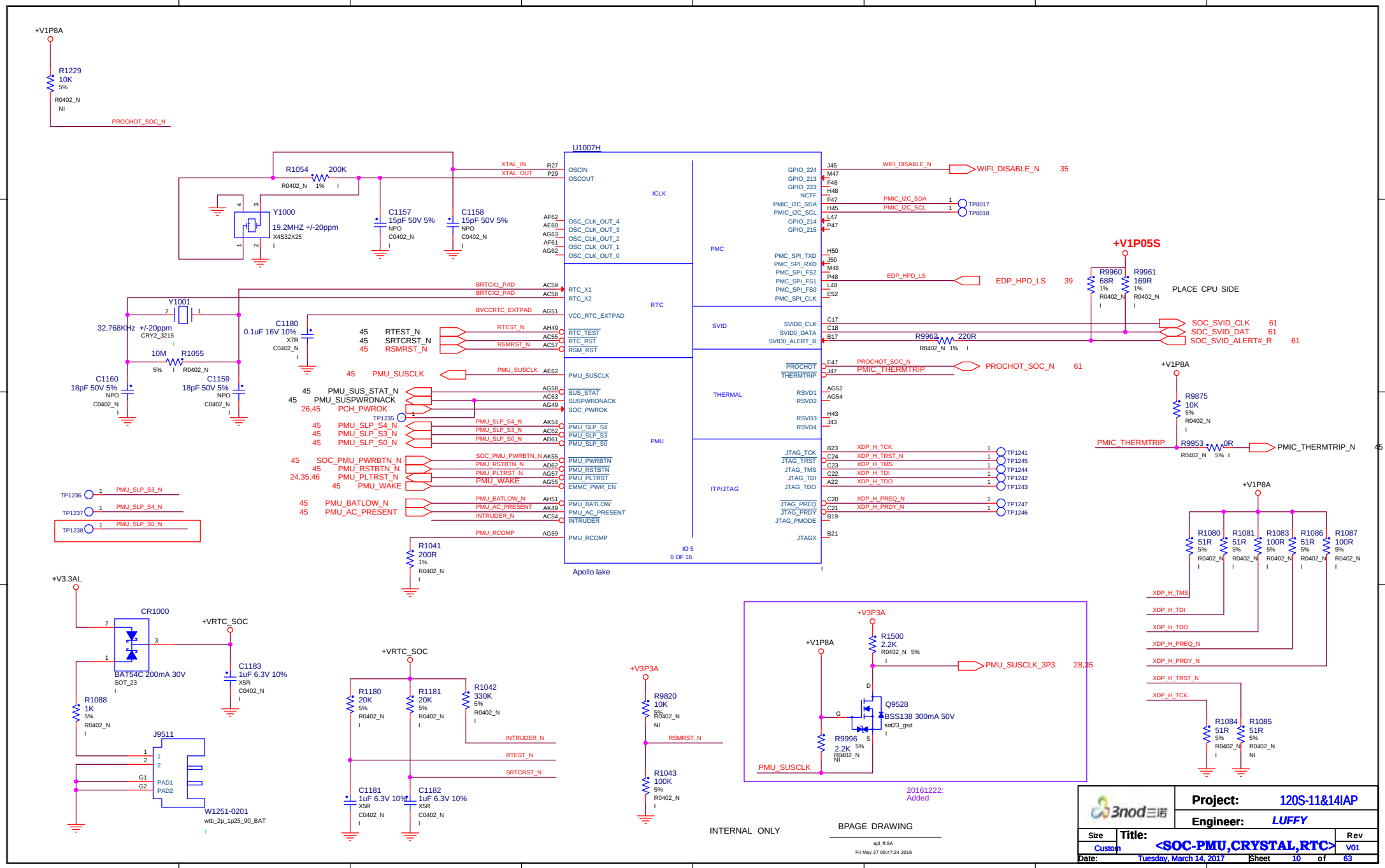

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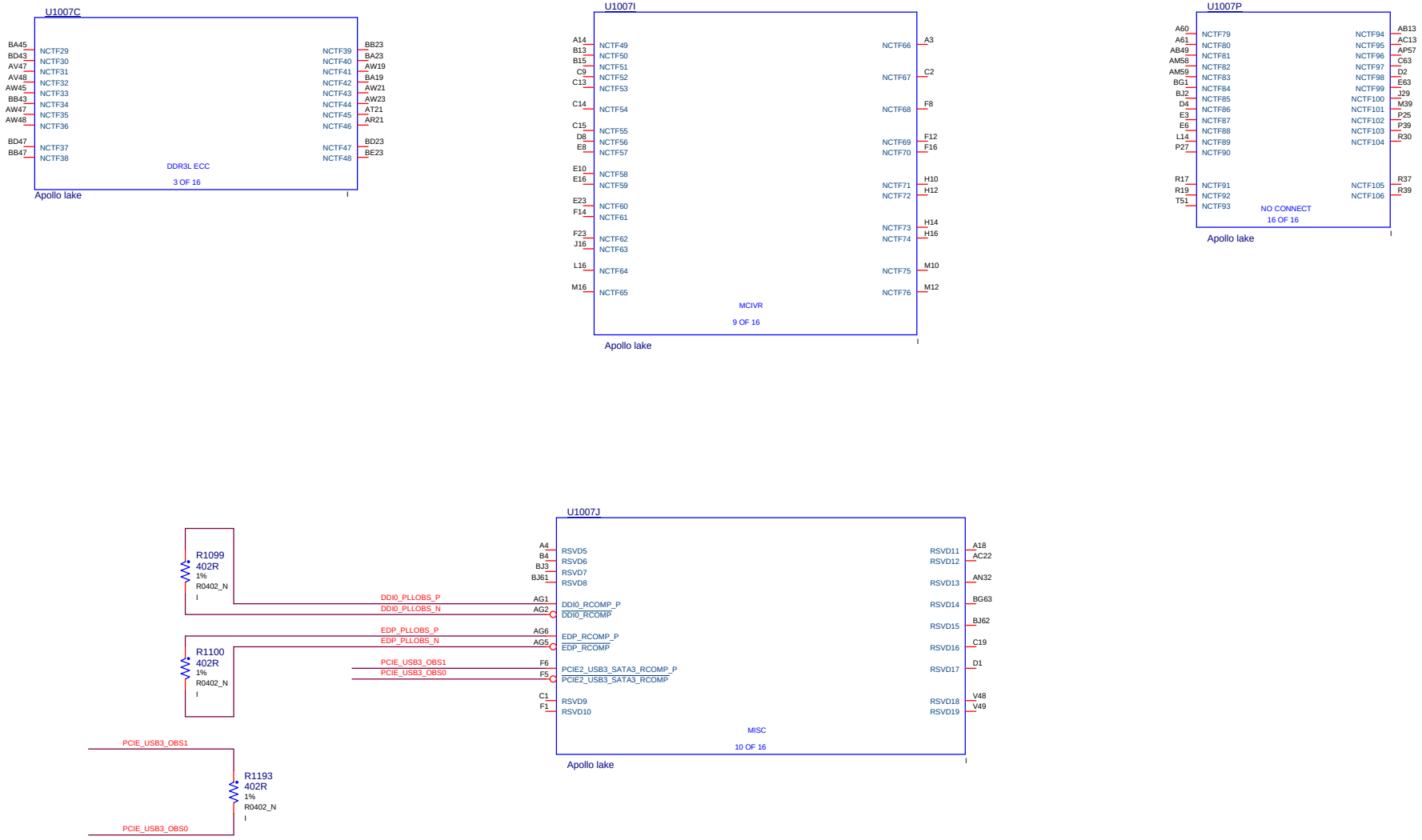

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apl_ff.8A
Fri May 27 06:47:24 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <SOC-MISC>	Rev: V01
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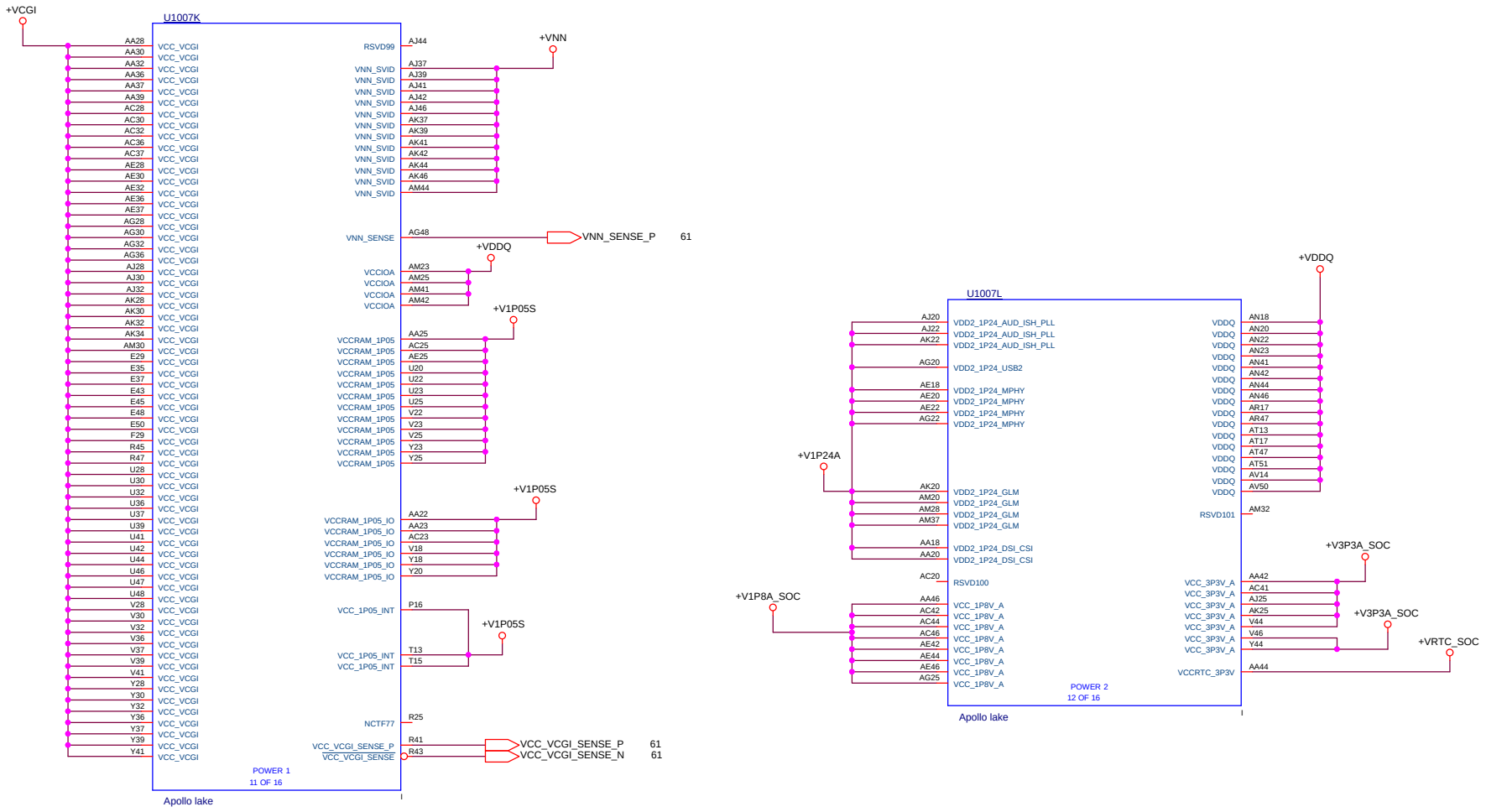
SOC: POWER



BPAGE DRAWING

apl_ff.+V1P0.9
Fri May 27 06:47:14 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	SOC-POWER	Rev: V01
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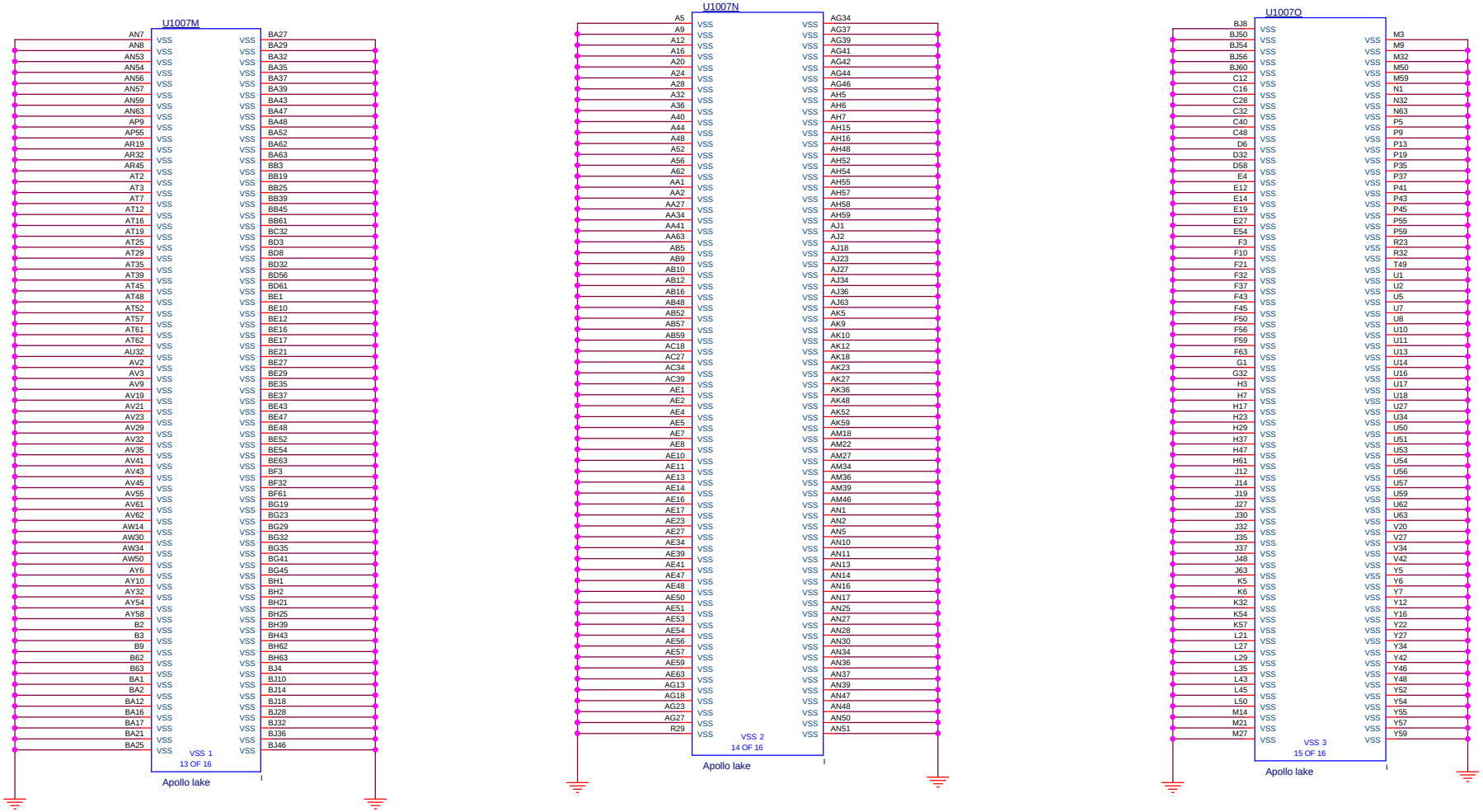
SOC: GND



BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:14 2016

3nod三诺	Project: 120S-11&14IAP	
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SOC: DECAPS

CAD NOTE:
PLACE IN BETWEEN SOC AND DRAM

+V1P8A_SOC — NOBOM JUMP_43X39 JUMP-SH1110 — +V1P8A

+V3P3A_SOC — NOBOM JUMP_43X39 JUMP-SH1111 — +V3P3A

+VDDQ

C1073 22uF 6.3V 20% X5R C0603_N I
C1081 22uF 6.3V 20% X5R C0603_N I
C1088 22uF 6.3V 20% X5R C0603_N I
C1093 22uF 6.3V 20% X5R C0603_N I
C1071 22uF 6.3V 20% X5R C0603_N I
C1075 22uF 6.3V 20% X5R C0603_N I
C1076 22uF 6.3V 20% X5R C0603_N I
C1078 22uF 6.3V 20% X5R C0603_N I

20161223"
Changed the footprint to 0603

+V1P8A_SOC — BSC
C1132 1uF 6.3V 10% X5R C0402_N I
C1135 1uF 6.3V 10% X5R C0402_N I
C1138 1uF 6.3V 10% X5R C0402_N I
C1140 1uF 6.3V 10% X5R C0402_N I
C1143 22uF 6.3V 20% X5R C0603_N I

+V3P3A_SOC — BSC
C1144 1uF 6.3V 10% X5R C0402_N I
C1145 1uF 6.3V 10% X5R C0402_N I
C1146 1uF 6.3V 10% X5R C0402_N I
C1215 1uF 6.3V 10% X5R C0402_N I
C1147 22uF 6.3V 20% X5R C0603_N I

+VDDQ — BSC
C1241 1uF 6.3V 10% X5R C0402_N I
C1242 1uF 6.3V 10% X5R C0402_N I

+V1P24A — BSC
C1108 1uF 6.3V 10% X5R C0402_N I
C1110 1uF 6.3V 10% X5R C0402_N I
C1112 1uF 6.3V 10% X5R C0402_N I
C1116 1uF 6.3V 10% X5R C0402_N I
C1119 1uF 6.3V 10% X5R C0402_N I
C1123 1uF 6.3V 10% X5R C0402_N I
C1127 1uF 6.3V 10% X5R C0402_N I
C1131 1uF 6.3V 10% X5R C0402_N I

C1109 1uF 6.3V 10% X5R C0402_N I
C1111 1uF 6.3V 10% X5R C0402_N I
C1113 1uF 6.3V 10% X5R C0402_N I
C1118 1uF 6.3V 10% X5R C0402_N I
C1126 22uF 6.3V 20% X5R C0603_N I
C1130 22uF 6.3V 20% X5R C0603_N I
C1134 22uF 6.3V 20% X5R C0603_N I
C1137 22uF 6.3V 20% X5R C0603_N I

+VNN — BSC
C1235 1uF 6.3V 10% X5R C0402_N I
C1086 1uF 6.3V 10% X5R C0402_N I
C1092 1uF 6.3V 10% X5R C0402_N I
C1097 1uF 6.3V 10% X5R C0402_N I

+VNN
C1114 1uF 6.3V 10% X5R C0402_N I

C1236 22uF 6.3V 20% X5R C0603_N I
C1087 22uF 6.3V 20% X5R C0603_N I
C1082 22uF 6.3V 20% X5R C0603_N I
C1083 22uF 6.3V 20% X5R C0603_N I
C1094 22uF 6.3V 20% X5R C0603_N I
C1098 22uF 6.3V 20% X5R C0603_N I

+VRTC_SOC
C1142 1uF 6.3V 10% X5R C0402_N I

CAD NOTE: C1142 PLACE CLOSE TO PIN AA44

+VCGI — BSC
C1067 1uF 6.3V 10% X5R C0402_N I
C1069 1uF 6.3V 10% X5R C0402_N I
C1074 1uF 6.3V 10% X5R C0402_N I
C1079 1uF 6.3V 10% X5R C0402_N I
C1085 1uF 6.3V 10% X5R C0402_N I
C1091 1uF 6.3V 10% X5R C0402_N I
C1096 1uF 6.3V 10% X5R C0402_N I
C1100 1uF 6.3V 10% X5R C0402_N I
C1102 1uF 6.3V 10% X5R C0402_N I
C1104 1uF 6.3V 10% X5R C0402_N I
C1105 1uF 6.3V 10% X5R C0402_N I
C1214 1uF 6.3V 10% X5R C0402_N I

C1068 22uF 6.3V 20% X5R C0603_N I
C1089 22uF 6.3V 20% X5R C0603_N I
C1095 22uF 6.3V 20% X5R C0603_N I
C1099 22uF 6.3V 20% X5R C0603_N I
C1103 22uF 6.3V 20% X5R C0603_N I

MLCC

20170323 Deleted C1072,C1077,C1084

20170323 Deleted C1169

20170207 Changed to NI;
20170210 Deleted C1007/C1015

C1148 1uF 6.3V 10% X5R C0402_N I
C1149 1uF 6.3V 10% X5R C0402_N I

+V1P05S
C1117 1uF 6.3V 10% X5R C0402_N I
C1121 1uF 6.3V 10% X5R C0402_N I
C1125 1uF 6.3V 10% X5R C0402_N I
C1129 1uF 6.3V 10% X5R C0402_N I
C1133 22uF 6.3V 20% X5R C0603_N I
C1136 22uF 6.3V 20% X5R C0603_N I
C1139 22uF 6.3V 20% X5R C0603_N I

BSC
C1115 1uF 6.3V 10% X5R C0402_N I
C1120 1uF 6.3V 10% X5R C0402_N I
C1124 1uF 6.3V 10% X5R C0402_N I
C1128 1uF 6.3V 10% X5R C0402_N I

BPAGE DRAWING
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Fri May 27 06:47:16 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: SOC-(DECAP)	Rev: V01
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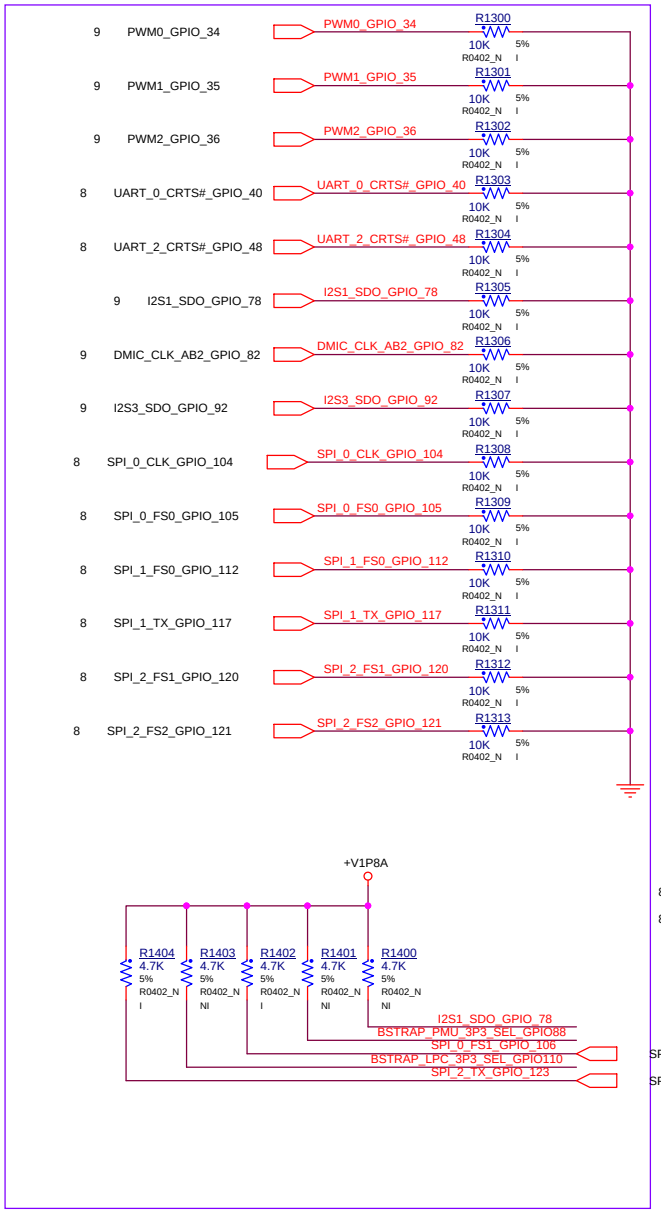
SOC: 7 OF 12



20161220:
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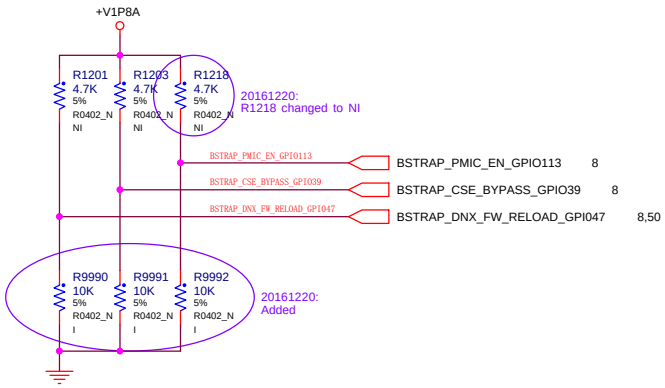

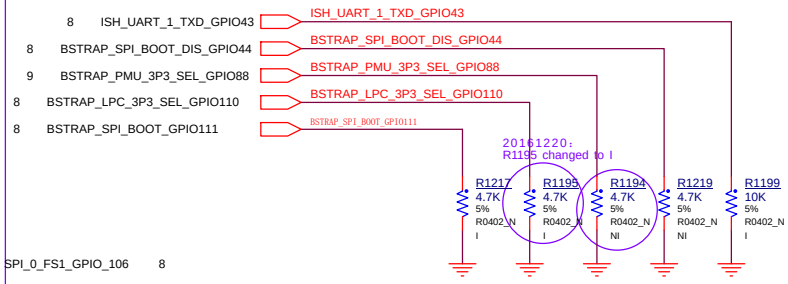

BSTRAP_LPC_3P3_SEL: LPC 1V8/3V3 mode select(20K PU)
1=buffers set to 1V8 mode(default)
0=buffers set to 3v3 mode(default)

BXT-P GPIO	SOC Ball Name	BSTRAP	Default Internal PU/PD
GPIO34	PWM0	Delayed_vref_switch) 0= not delayed(Default) 1=delayed	PD
GPIO35	PWM1	Spare1 0= do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO36	PWM2	Spare2 0 =VDD2 IS 1.24V(Default) 1=VDD2 IS 1.35V	PD
GPIO39	LPASS_UART0_TXD	Eable CSE ROM bypass 0 = disable bypass (default) 1 = enable bypass	PD
GPIO40	RTC Clock Timer Bypass	RTC Clock Timer Bypass 0 =disable bypass (Default) 1 =enable bypass	PD
GPIO43	LPASS_UART1_TXD	Select eMMC boot source 0 =do now allow (Default) 1=allow	PU
GPIO44	LPASS_UART1_RTS_B	Select SPI boot source 0 =Disable 1=Enable(Default)	PU
GPIO47	LPASS_UART2_TXD	Force DNX FW Load 0 =Disable(Default) 1=Enable	PD
GPIO48	LPASS_UART2_RTS_B	LPC Boot strap 0 =Do not boot from LPC(Default) 1=Enable	PD
GPIO78	AVS_I2S1_SDO	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO82	AVS_M_CLK_AB2	WC_PRESENT 0=non-Whiskey Cove(Default) 1=Whiskey Cove is connected	PD
GPIO88	AVS_I2S2_SD0	PMU (Power Management Unit) 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO92	AVS_I2S3_SD0	SMBus No Re-Boot 0=Dsiable(Default) 1=Enable	PD
GPIO104	GP_SSP_0_CLK	(HVM Tester)XTAL startup 0=Dsiable(Default) 1=Enable	PD
GPIO105	GP_SSP_0_FS0	(HVM Tester)XTAL startup 0=Dsiable(Default) 1=Enable	PU
GPIO106	GP_SSP_0_FS1	Halts early boot for debug 0=Enable 1=Disable	PU
GPIO110	GP_SSP_0_TXD	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO111	GP_SSP_1_CLK	SPI Boot BIOS strap 0=boot from SPI(Debug) 1=Do not boot from SPI (default)	PU
GPIO112	GP_SSP_1_FS0	Enable metal password auth 0=Disable 1=Enable	PD
GPIO113	GP_SSP_1_FS1	SVID diable 0=Enable SVID(Default) 1=Disbale SVID	PU
GPIO117	GP_SSP_1_TXD	Stall BOot FSM for debut 0=Do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO118	GP_SSP_2_CLK	Flash Descriptpr Override Pin-Strao status 0=Disable(Default) 1=Enable	PD
GPIO120	GP_SSP_2_FS1	Top swap pverride 0=Disable(Default) 1=Enable	PD
GPIO121	GP_SSP_2_FS2	Plled LOW when RSM_RST_N deasserts	PD
GPIO123	GP_SSP_2_TXD	Pulled HIGH when RSM_RST_N de-asserts	PU

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
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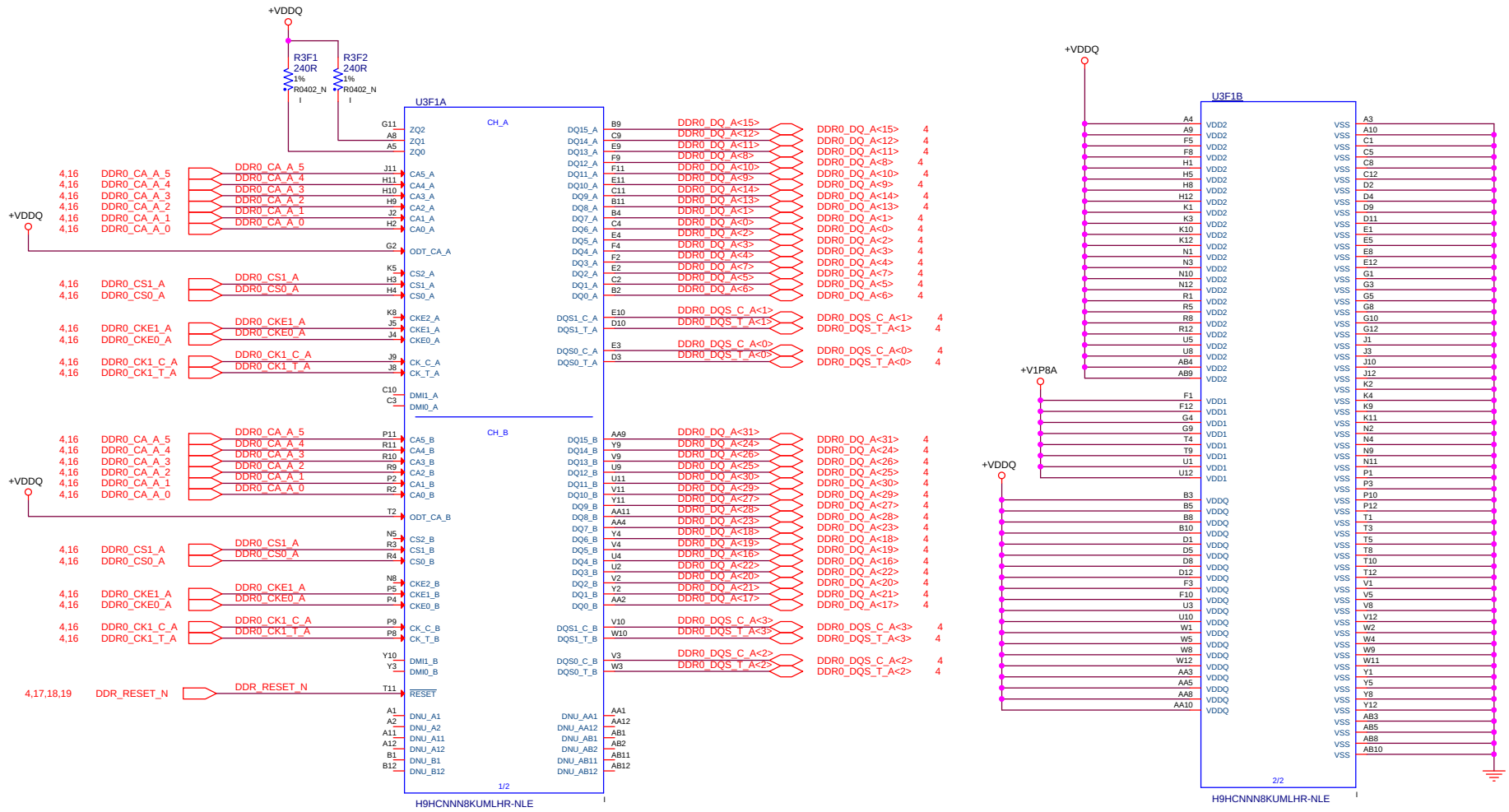
CHANNEL 0 - MEMORY1/2



BPAGE DRAWING

apl_lf.GND
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	MEM_LPDDR4 CH0-1 of 2	Rev: V01
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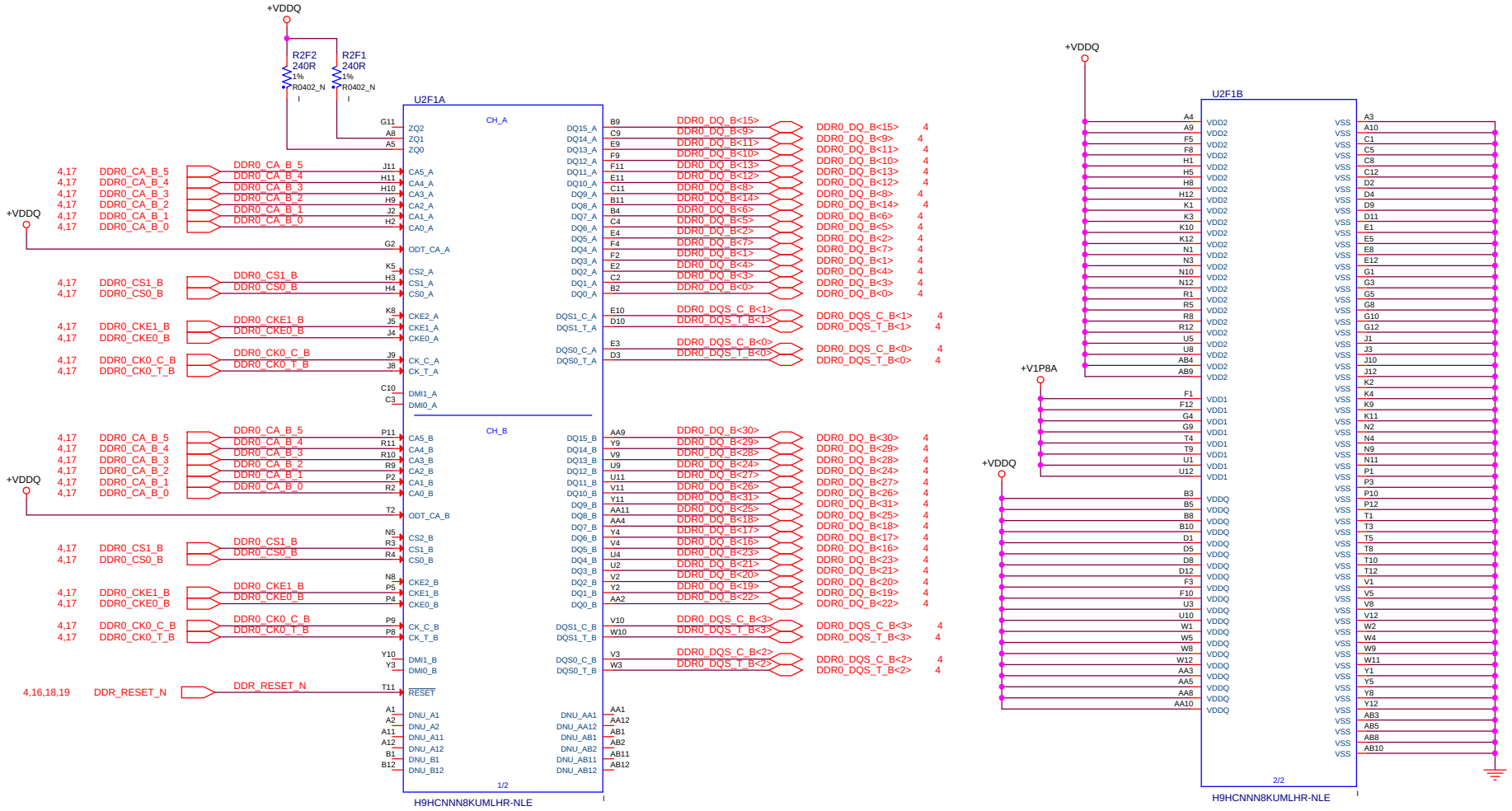
CHANNEL 0 - MEMORY2/2



BPAGE DRAWING

apl_ff.GND

Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	MEM_LPDDR4 CH0-2 of 2	Rev: V01
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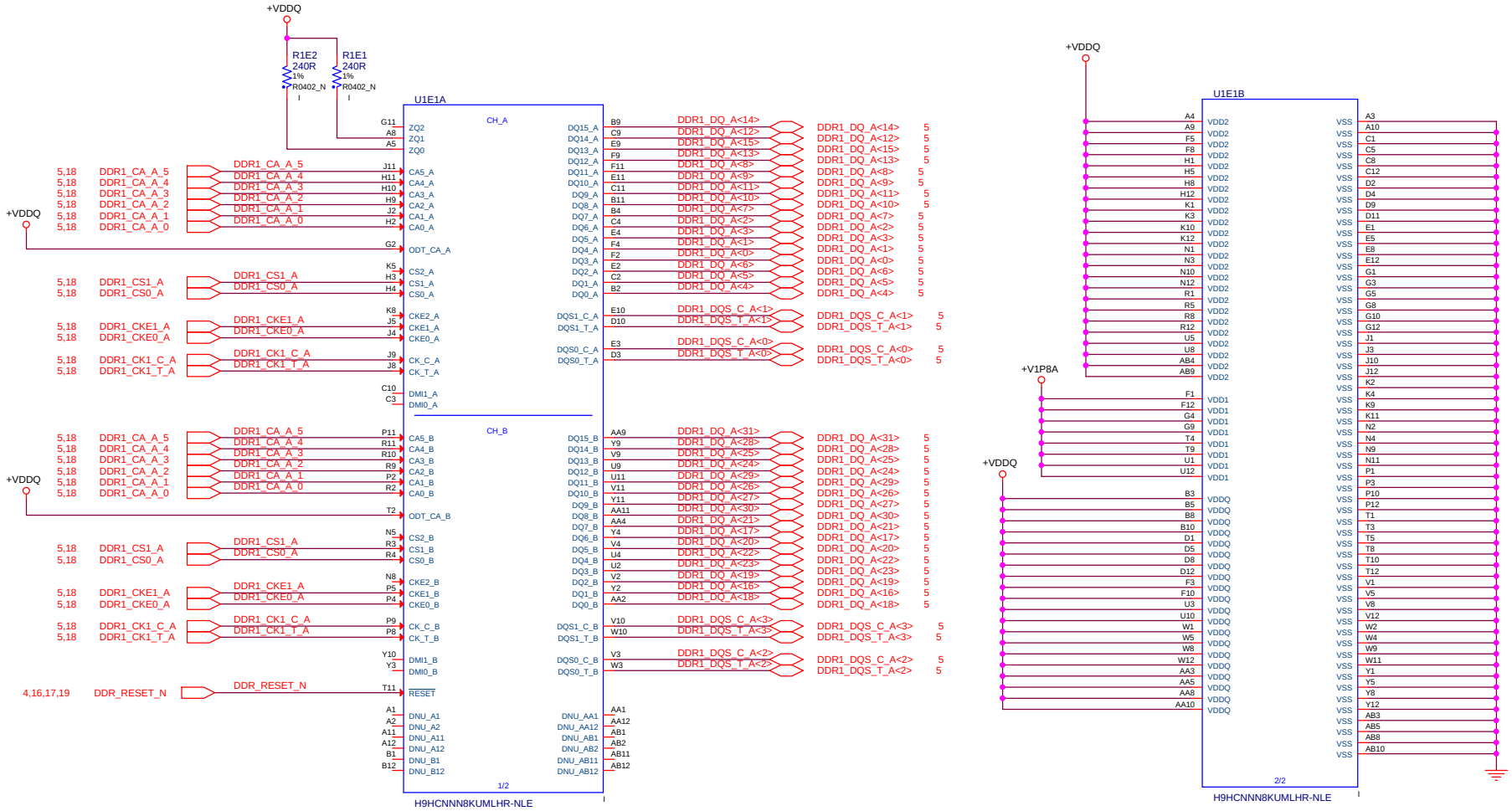
CHANNEL 1 - MEMORY1/2



BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	MEM_LPDDR4 CH1-1 of 2
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 18 of 63	

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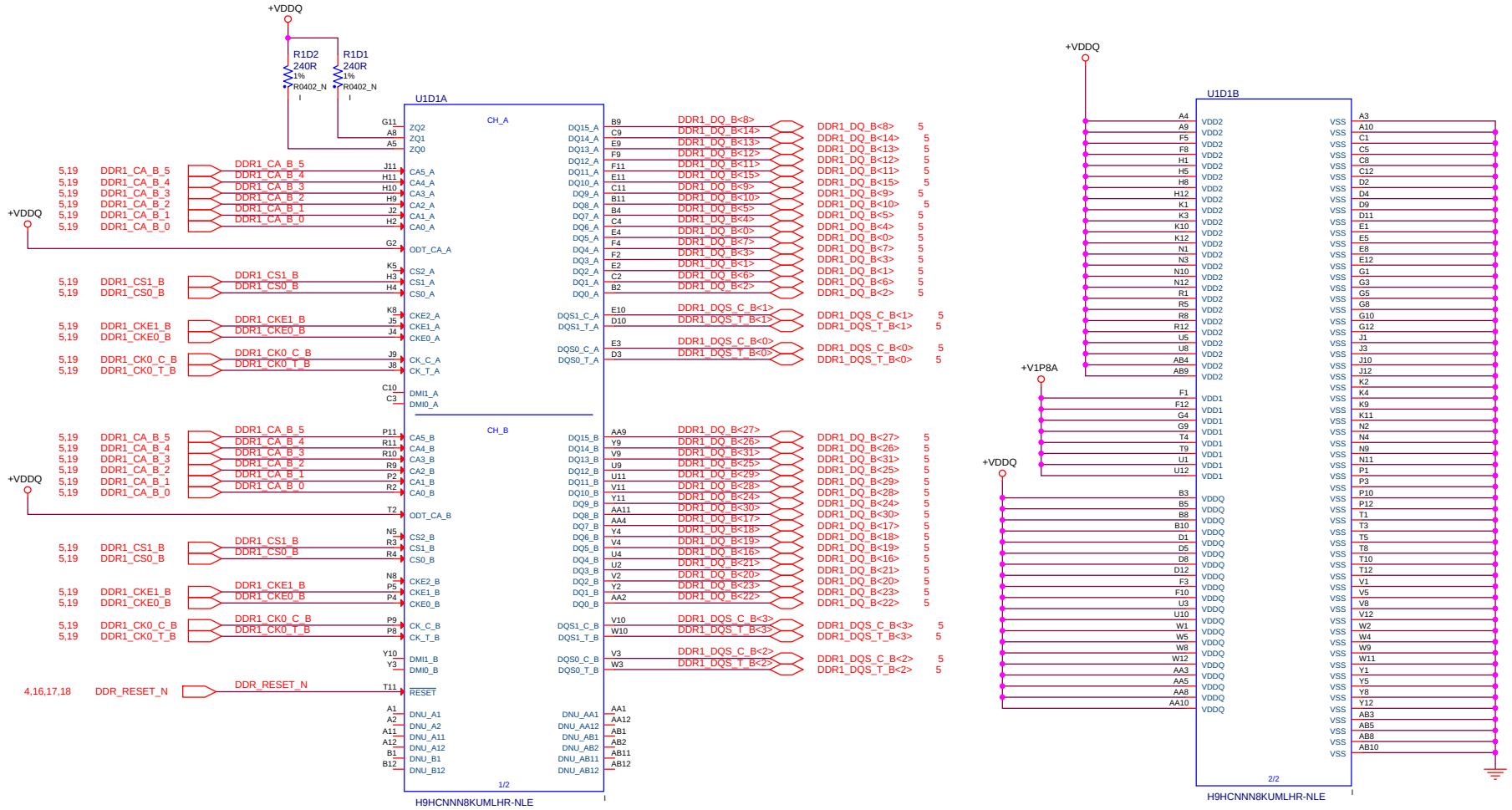
CHANNEL 1 - MEMORY2/2



BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:18 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: MEM_LPDDR4 CH1-2of 2	Rev: V01
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BPAGE DRAWING

apl_ff.+V1P8.18
Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: NC	Rev: V01
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BPAGE DRAWING

apl_ff.+V1P8.18
Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	*LUFFY*
Size: Custom	Title: NC	Rev: V01
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BPAGE DRAWING

apl_ff.8A

Fri May 27 06:47:18 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: MEM_LPDDR4-DECAPS	Rev: V01
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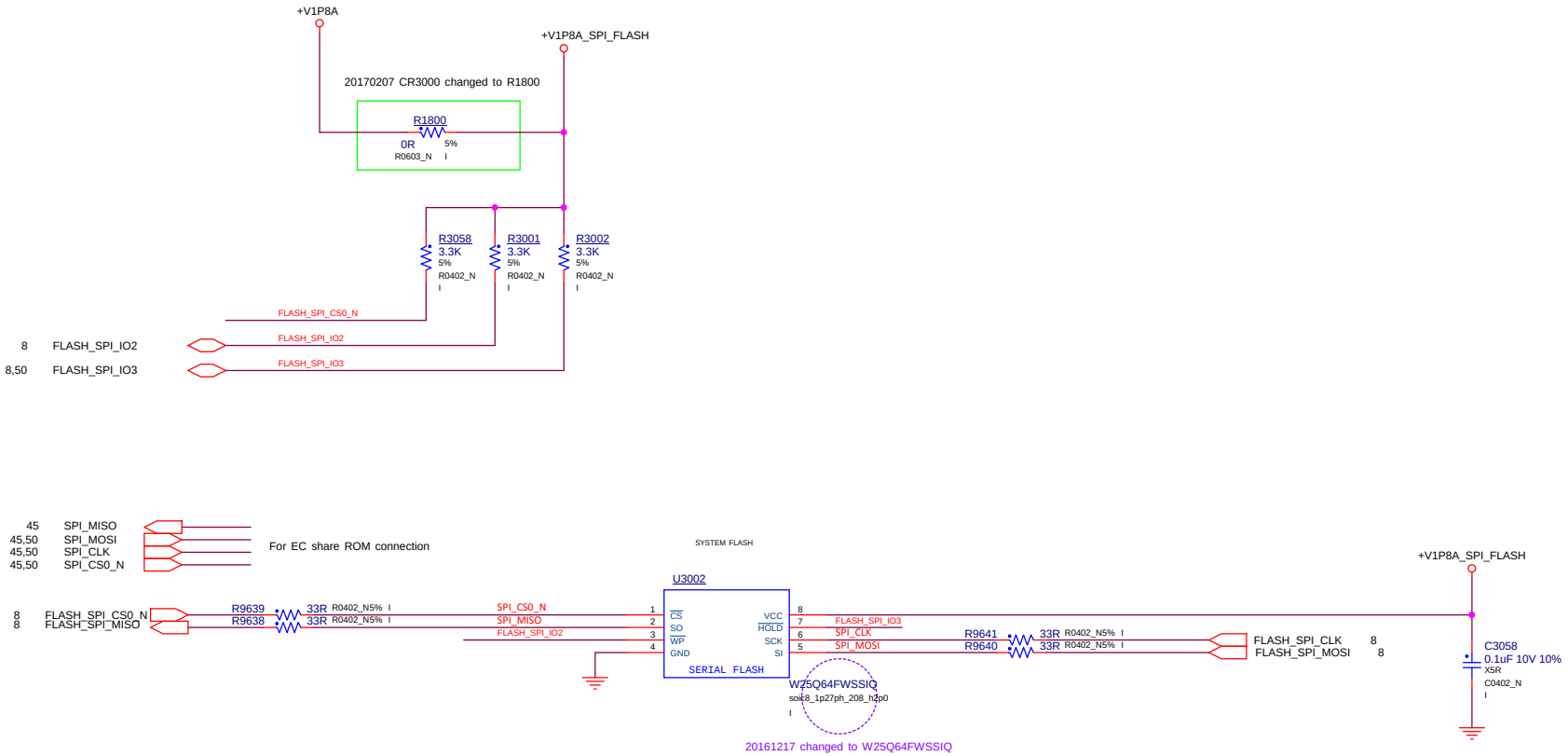
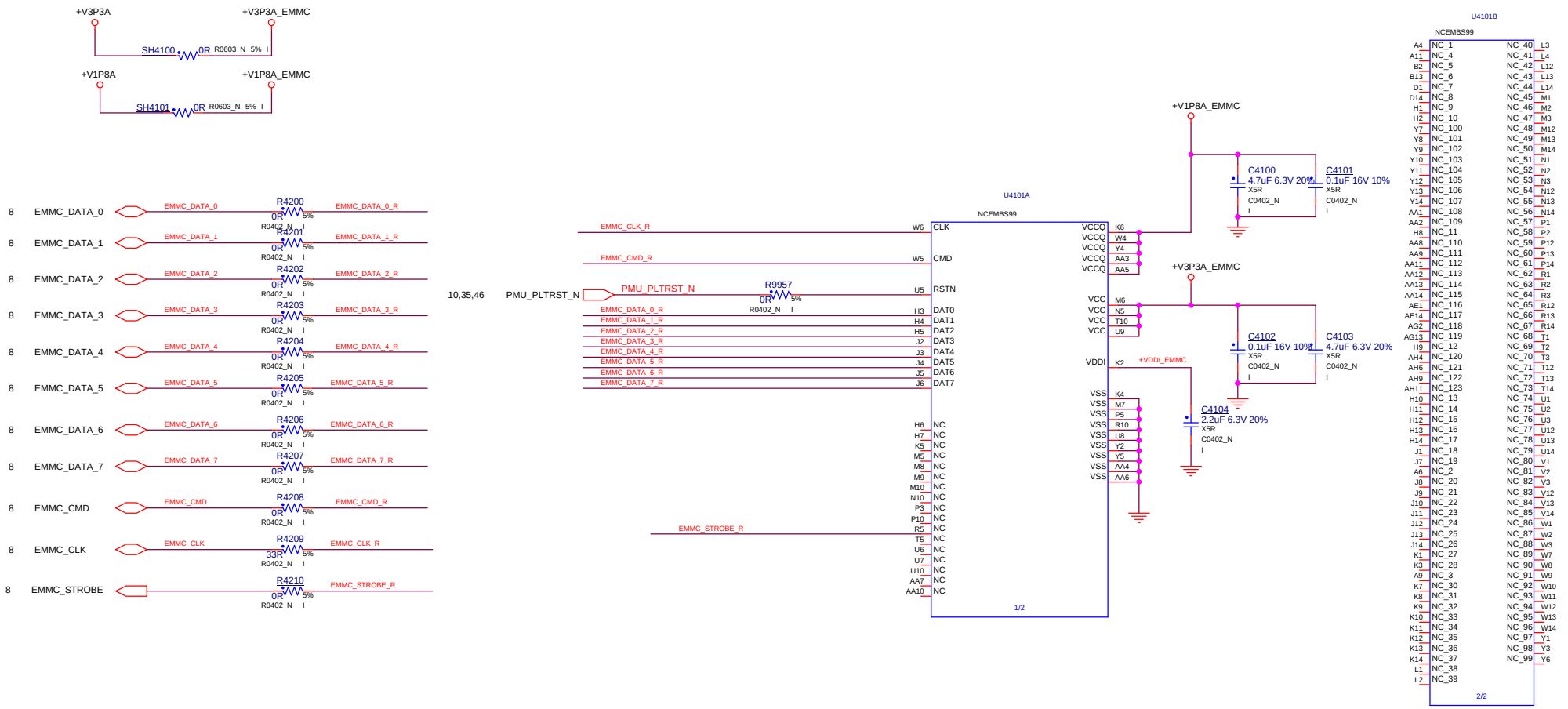


INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:20 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <SYSTEM_FLASH>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 23 of 63	



INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:20 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <EMMC>	Rev: V01
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apl_ff.s
Fri May 27 06:47:20 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
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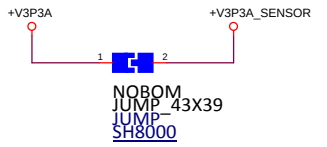
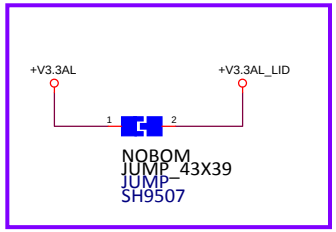
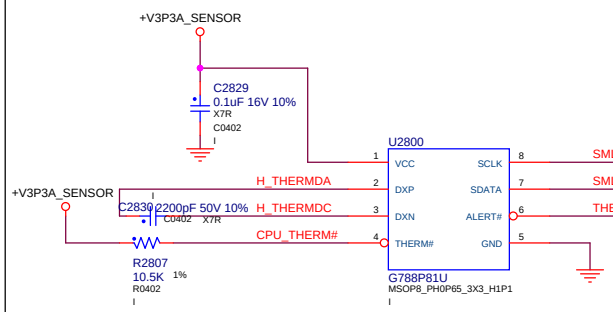
SENSORS

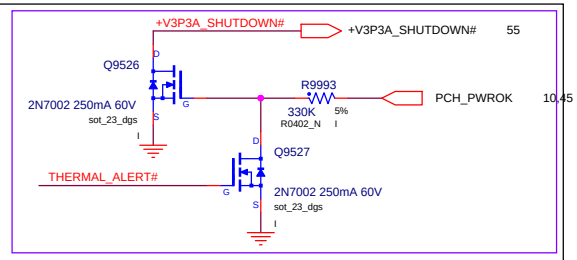




20170316 Added

CPU THERMAL SENSOR





20161220 :Added

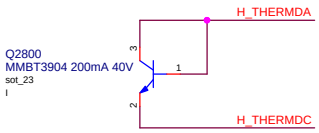
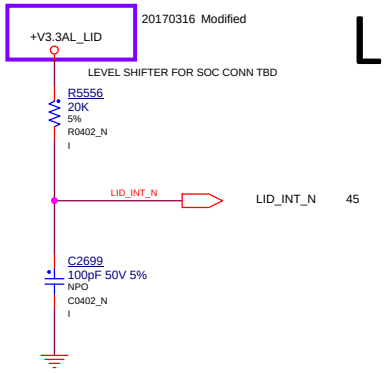


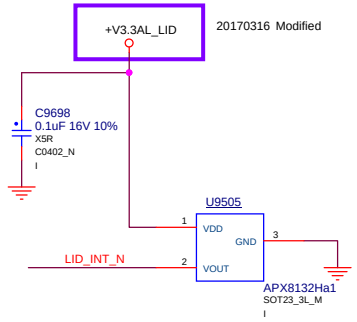
Table 10. Remote temperature $\overline{\text{THERM}}$ limit

The default value is trapping after power up 100ms by different pull-up resistors of $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ pin:

TEMPERATURE (°C)		$\overline{\text{THERM}}$				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

LID SENSOR





INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:20 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <SENSORS>	Rev: V01
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BPAGE DRAWING

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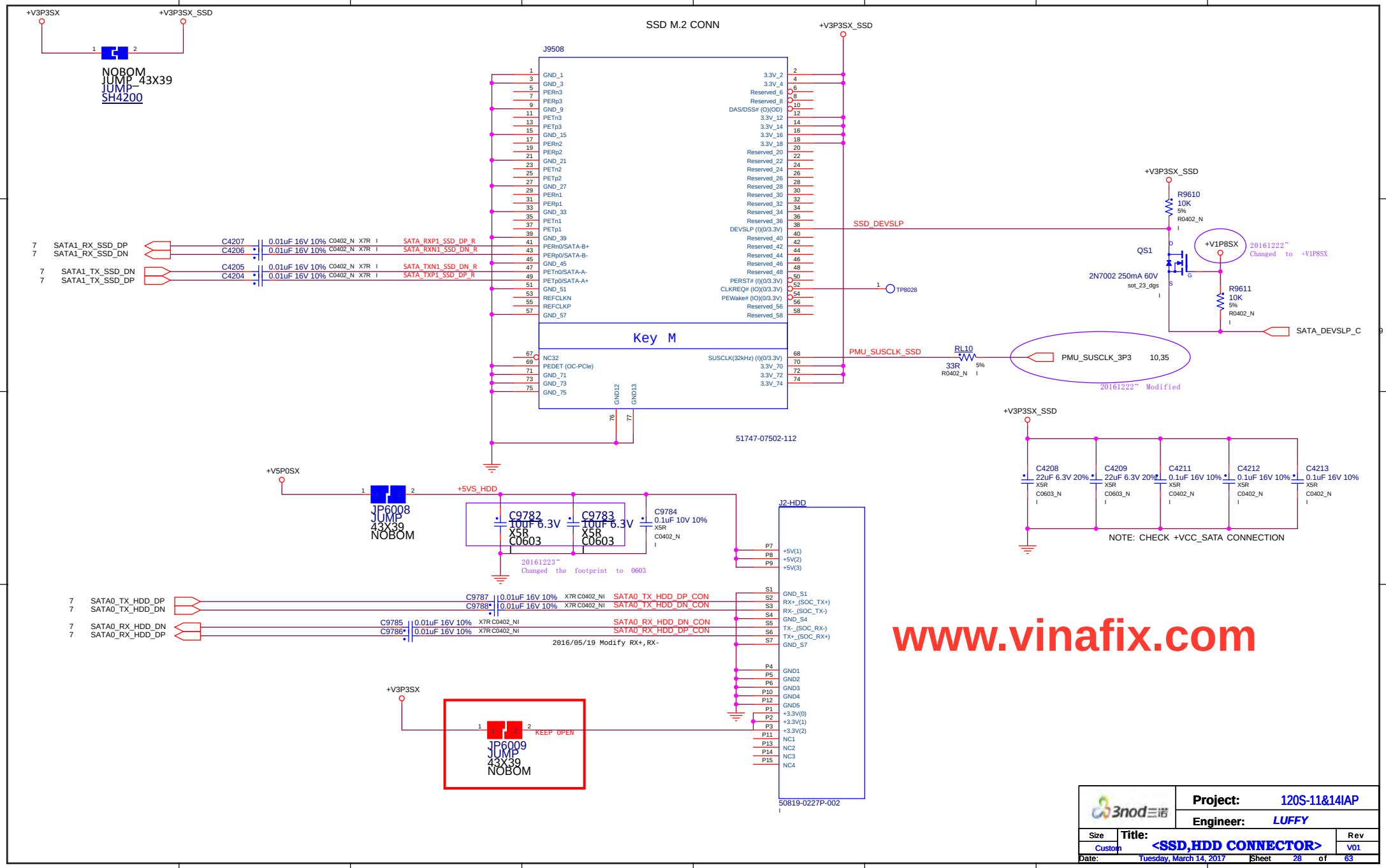
Fri May 27 06:47:22 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 27 of 63	



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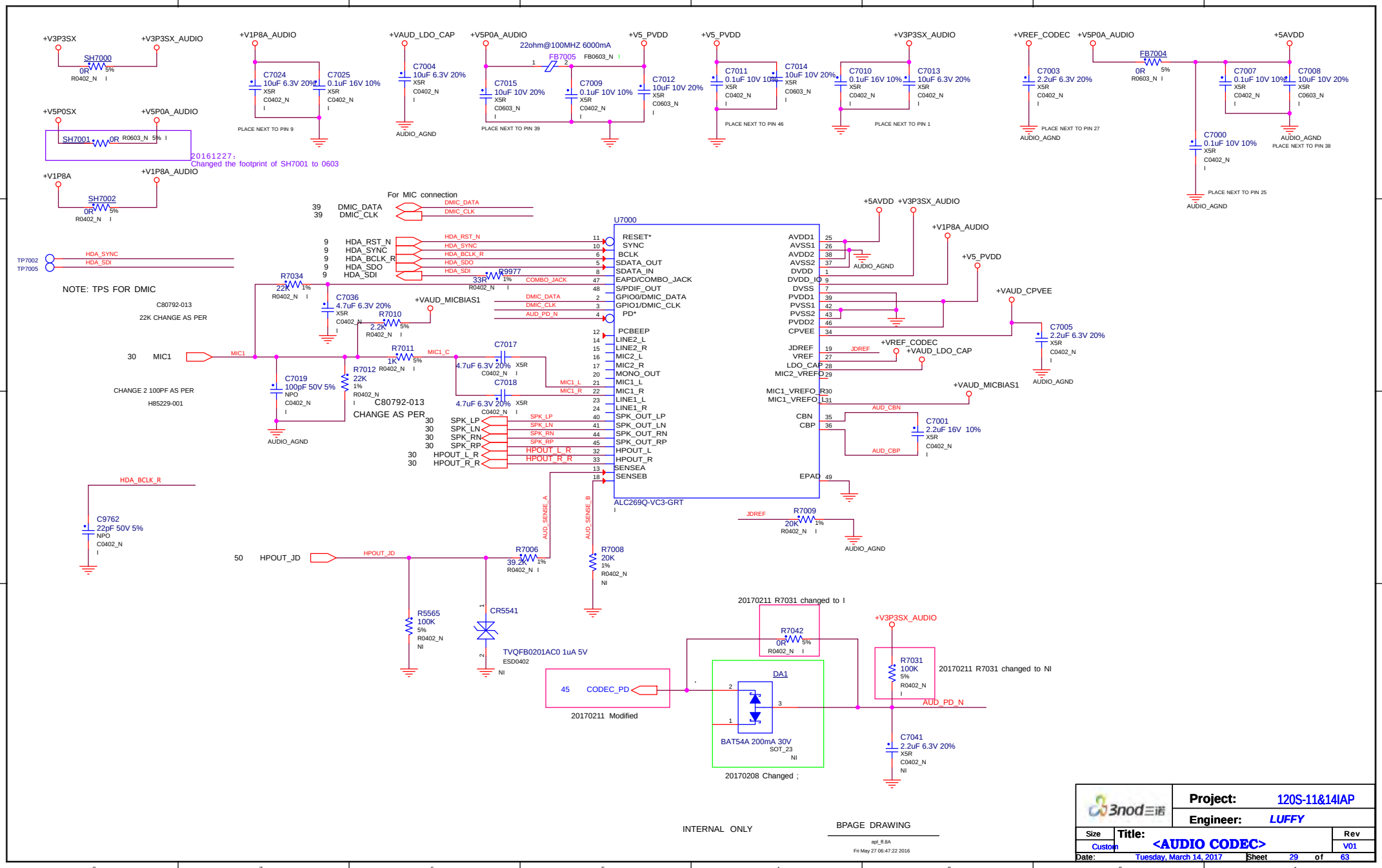
+V3P3SX
+V3P3SX_AUDIO
SH7000
0R
R0402_N
+V1P8A_AUDIO
C7024
10uF 6.3V 20%
C7025
0.1uF 16V 10%
C0402_N
PLACE NEXT TO PIN 9
+VAUD_LDO_CAP
C7004
10uF 6.3V 20%
AUDIO_AGND
+V5P0A_AUDIO
22ohm@100MHZ 6000mA
FB7005
FB0603_N
C7015
10uF 10V 20%
C0603_N
PLACE NEXT TO PIN 39
C7009
0.1uF 10V 10%
+V5_PVDD
C7012
10uF 10V 20%
C7011
0.1uF 10V 10%
C7014
10uF 10V 20%
PLACE NEXT TO PIN 46
C7010
0.1uF 16V 10%
C7013
10uF 6.3V 20%
PLACE NEXT TO PIN 1
+VREF_CODEC
C7003
2.2uF 6.3V 20%
PLACE NEXT TO PIN 27
+5AVDD
FB7004
R0603_N
C7007
0.1uF 10V 10%
C7008
10uF 10V 20%
C7000
0.1uF 10V 10%
PLACE NEXT TO PIN 25
PLACE NEXT TO PIN 38
+V5P0SX
SH7001
R0603_N
20161227:
Changed the footprint of SH7001 to 0603
+V1P8A
SH7002
For MIC connection
39 DMIC_DATA
39 DMIC_CLK
U7000
RESET*
SYNC
BCLK
SDATA_OUT
SDATA_IN
EAPD/COMBO_JACK
S/PDIF_OUT
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD*
PCBEEP
LINE2_L
LINE2_R
MIC2_L
MIC2_R
MONO_OUT
MIC1_L
MIC1_R
LINE1_L
LINE1_R
SPK_OUT_LP
SPK_OUT_LN
SPK_OUT_RN
SPK_OUT_RP
HPOUT_L
HPOUT_R
SENSEA
SENSEB
AVDD1
AVSS1
AVDD2
AVSS2
DVDD
DVDD_IO
DVSS
PVDD1
PVSS1
PVSS2
PVDD2
CPVEE
JDREF
VREF
LDO_CAP
MIC2_VREFO
MIC1_VREFO_R
MIC1_VREFO_L
CBN
CBP
EPAD
ALC269Q-VC3-GRT
+5AVDD
+V3P3SX_AUDIO
+V1P8A_AUDIO
+V5_PVDD
+VAUD_CPVEE
C7005
2.2uF 6.3V 20%
+VREF_CODEC
+VAUD_LDO_CAP
+VAUD_MICBIAS1
C7001
2.2uF 16V 10%
AUD_CBN
AUD_CBP
R7009
20K
HDA_RST_N
HDA_SYNC
HDA_BCLK_R
HDA_SDO
HDA_SDI
R9977
33R
COMBO_JACK
DMIC_DATA
DMIC_CLK
AUD_PD_N
TP7002
TP7005
NOTE: TPS FOR DMIC
C80792-013
22K CHANGE AS PER
R7034
22K
C7036
4.7uF 6.3V 20%
R7010
2.2K
30 MIC1
MIC1
R7011
1K
MIC1_C
C7017
4.7uF 6.3V 20%
C7018
4.7uF 6.3V 20%
MIC1_L
MIC1_R
CHANGE 2 100PF AS PER
H85229-001
C7019
100pF 50V 5%
R7012
22K
C80792-013
CHANGE AS PER
30 SPK_LP
30 SPK_LN
30 SPK_RN
30 SPK_RP
30 HPOUT_L_R
30 HPOUT_R_R
SPK_LP
SPK_LN
SPK_RN
SPK_RP
HPOUT_L_R
HPOUT_R_R
HDA_BCLK_R
C9762
22pF 50V 5%
AUD_SENSE_A
AUD_SENSE_B
50 HPOUT_JD
HPOUT_JD
R7006
39.2K
R7008
20K
R5565
100K
CR5541
TVQFB0201AC0 1uA 5V
ESD0402
20170211 R7031 changed to I
R7042
0R
+V3P3SX_AUDIO
R7031
100K
20170211 R7031 changed to NI
45 CODEC_PD
20170211 Modified
DA1
BAT54A 200mA 30V
SOT_23
20170208 Changed ;
AUD_PD_N
C7041
2.2uF 6.3V 20%
INTERNAL ONLY
BPAGE DRAWING
apl_ll.8A
Fri May 27 06:47:22 2016
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: <AUDIO CODEC>
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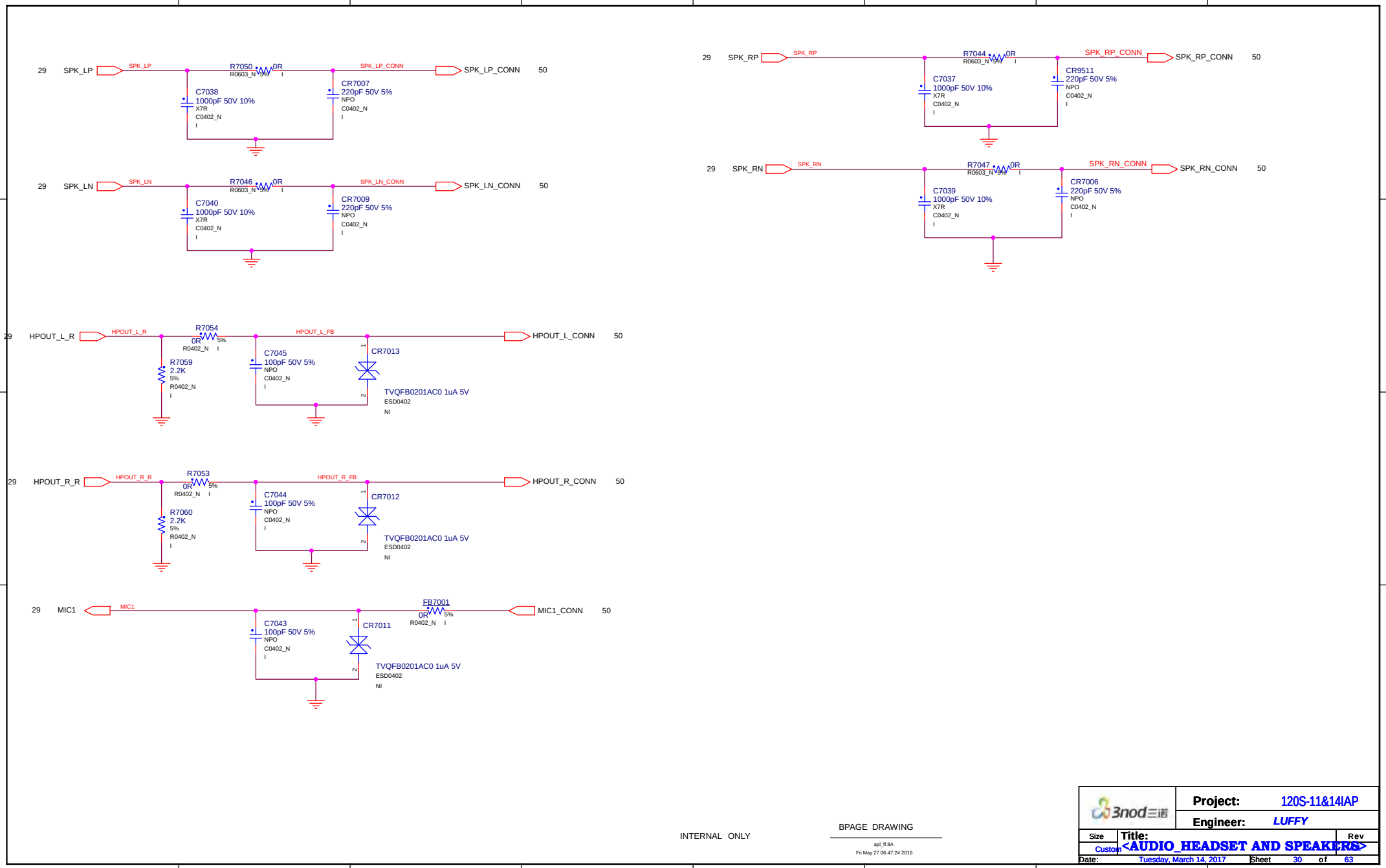

INTERNAL ONLY

BPAGE DRAWING

apl_ff.8A
Fri May 27 06:47:24 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: *LUFFY*	
Size: Custom	Title: <AUDIO_HEADSET AND SPEAKERS>	Rev
Date: Tuesday, March 14, 2017	Sheet 30 of 63	

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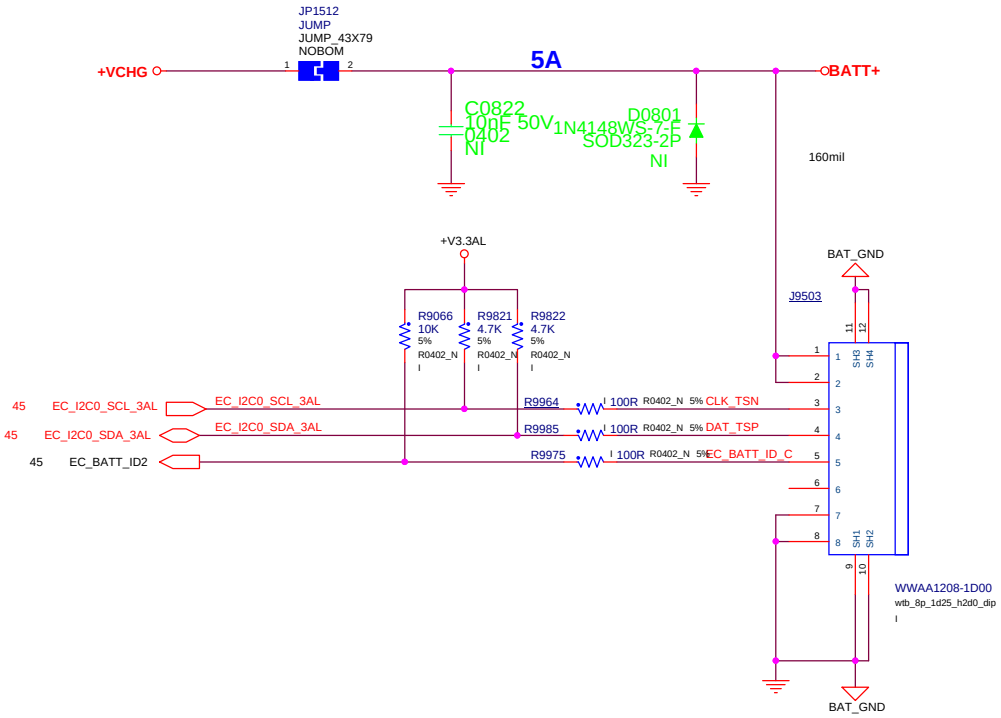
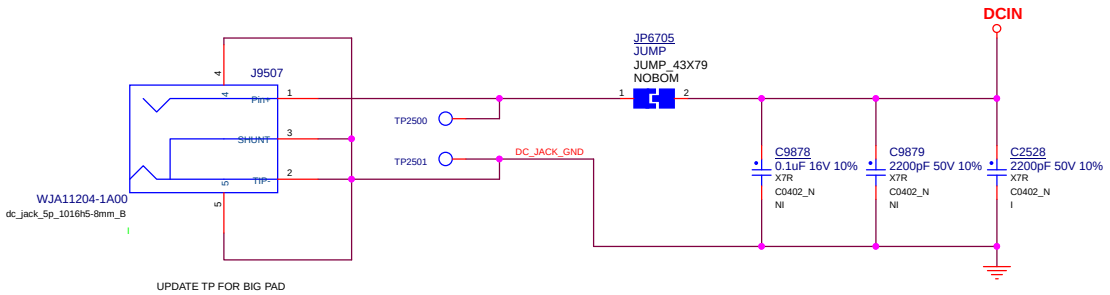


20170205 Deleted reserved design for dummy battery

3nod三诺	Project: 120S-11&14IAP	
	Engineer: GGS	
Size: Custom	Title: <GAUGE&BATTERY CONN>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 31 of 63	



UPDATE TP FOR BIG PAD

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BPAGE DRAWING

apl_ff.ADP_P.48
Fri May 27 06:47:24 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: GGS	
Size: Custom	Title: <DC JACK>	Rev: V01
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BPAGE DRAWING

apl_ff.8A
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3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
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apl_ff.
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TYPE-C PD CONTROLLER

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	Engineer: LUFFY	
Size: Custom	Title: <NC>	Rev: V01
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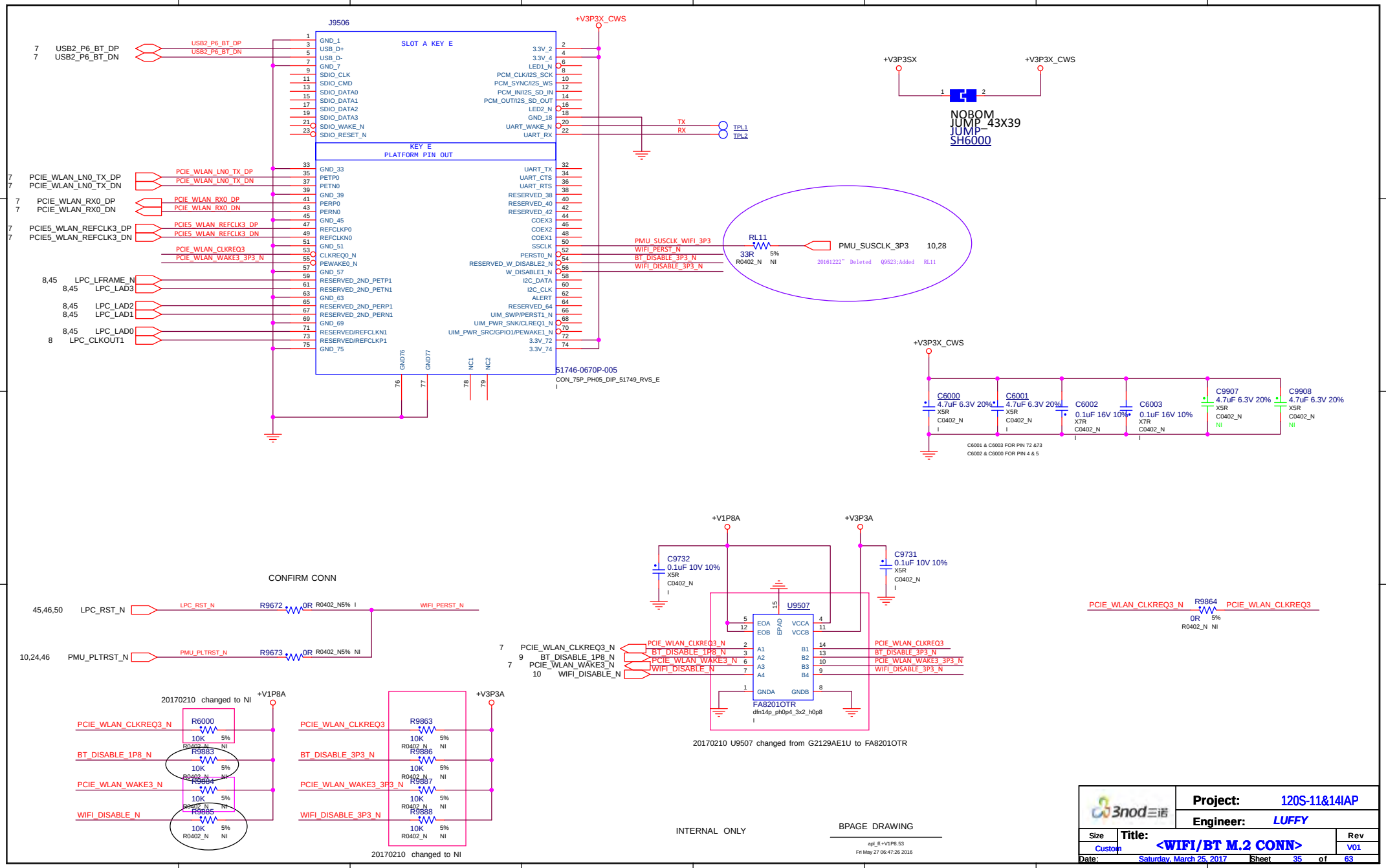
J9506
SLOT A KEY E
KEY E
PLATFORM PIN OUT
+V3P3X_CWS
7 USB2_P6_BT_DP
7 USB2_P6_BT_DN
USB2_P6_BT_DP
USB2_P6_BT_DN
GND_1
USB_D+
USB_D-
GND_7
SDIO_CLK
SDIO_CMD
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
SDIO_WAKE_N
SDIO_RESET_N
3.3V_2
3.3V_4
LED1_N
PCM_CLK/I2S_SCK
PCM_SYNC/I2S_WS
PCM_IN/I2S_SD_IN
PCM_OUT/I2S_SD_OUT
LED2_N
GND_18
UART_WAKE_N
UART_RX
TX
RX
TPL1
TPL2
+V3P3SX
+V3P3X_CWS
NOBOM
JUMP_43X39
JUMP
SH6000
7 PCIE_WLAN_LN0_TX_DP
7 PCIE_WLAN_LN0_TX_DN
PCIE_WLAN_LN0_TX_DP
PCIE_WLAN_LN0_TX_DN
7 PCIE_WLAN_RX0_DP
7 PCIE_WLAN_RX0_DN
PCIE_WLAN_RX0_DP
PCIE_WLAN_RX0_DN
7 PCIE5_WLAN_REFCLK3_DP
7 PCIE5_WLAN_REFCLK3_DN
PCIE5_WLAN_REFCLK3_DP
PCIE5_WLAN_REFCLK3_DN
PCIE_WLAN_CLKREQ3
PCIE_WLAN_WAKE3_3P3_N
8,45 LPC_LFRAME_N
8,45 LPC_LAD3
8,45 LPC_LAD2
8,45 LPC_LAD1
8,45 LPC_LAD0
8 LPC_CLKOUT1
GND_33
PETP0
PETN0
GND_39
PERP0
PERN0
GND_45
REFCLKP0
REFCLKN0
GND_51
CLKREQ0_N
PEWAKE0_N
GND_57
RESERVED_2ND_PETP1
RESERVED_2ND_PETN1
GND_63
RESERVED_2ND_PERP1
RESERVED_2ND_PERN1
GND_69
RESERVED/REFCLKN1
RESERVED/REFCLKP1
GND_75
UART_TX
UART_CTS
UART_RTS
RESERVED_38
RESERVED_40
RESERVED_42
COEX3
COEX2
COEX1
SSCLK
PERST0_N
RESERVED_W_DISABLE2_N
W_DISABLE1_N
I2C_DATA
I2C_CLK
ALERT
RESERVED_64
UIM_SWP/PERST1_N
UIM_PWR_SNK/CLREQ1_N
UIM_PWR_SRC/GPIO1/PEWAKE1_N
3.3V_72
3.3V_74
GND76
GND77
NC1
NC2
51746-0670P-005
CON_75P_PH05_DIP_51749_RVS_E
PMU_SUSCLK_WIFI_3P3
WIFI_PERST_N
BT_DISABLE_3P3_N
WIFI_DISABLE_3P3_N
RL11
33R 5%
R0402_N NI
PMU_SUSCLK_3P3 10,28
20161222 Deleted Q9523;Added RL11
+V3P3X_CWS
C6000 4.7uF 6.3V 20% X5R C0402_N
C6001 4.7uF 6.3V 20% X5R C0402_N
C6002 0.1uF 16V 10% X7R C0402_N
C6003 0.1uF 16V 10% X7R C0402_N
C9907 4.7uF 6.3V 20% X5R C0402_N NI
C9908 4.7uF 6.3V 20% X5R C0402_N NI
C6001 & C6003 FOR PIN 72 &73
C6002 & C6000 FOR PIN 4 & 5
CONFIRM CONN
45,46,50 LPC_RST_N
LPC_RST_N
R9672 0R R0402_N5% I
WIFI_PERST_N
10,24,46 PMU_PLTRST_N
PMU_PLTRST_N
R9673 0R R0402_N5% NI
+V1P8A
+V3P3A
C9732 0.1uF 10V 10% X5R C0402_N
C9731 0.1uF 10V 10% X5R C0402_N
U9507
EOA
EOB
EPAD
VCCA
VCCB
A1
A2
A3
A4
B1
B2
B3
B4
GNDA
GNDB
FA8201OTR
dfn14p_ph0p4_3x2_h0p8
7 PCIE_WLAN_CLKREQ3_N
9 BT_DISABLE_1P8_N
7 PCIE_WLAN_WAKE3_N
10 WIFI_DISABLE_N
PCIE_WLAN_CLKREQ3_N
BT_DISABLE_1P8_N
PCIE_WLAN_WAKE3_N
WIFI_DISABLE_N
PCIE_WLAN_CLKREQ3
BT_DISABLE_3P3_N
PCIE_WLAN_WAKE3_3P3_N
WIFI_DISABLE_3P3_N
20170210 U9507 changed from G2129AE1U to FA8201OTR
PCIE_WLAN_CLKREQ3_N
R9864 0R 5% R0402_N NI
PCIE_WLAN_CLKREQ3
20170210 changed to NI
+V1P8A
R6000 10K 5% R0402_N NI
R9883 10K 5% R0402_N NI
R9884 10K 5% R0402_N NI
R9885 10K 5% R0402_N NI
PCIE_WLAN_CLKREQ3_N
BT_DISABLE_1P8_N
PCIE_WLAN_WAKE3_N
WIFI_DISABLE_N
+V3P3A
R9863 10K 5% R0402_N NI
R9886 10K 5% R0402_N NI
R9887 10K 5% R0402_N NI
R9888 10K 5% R0402_N NI
PCIE_WLAN_CLKREQ3
BT_DISABLE_3P3_N
PCIE_WLAN_WAKE3_3P3_N
WIFI_DISABLE_3P3_N
20170210 changed to NI
INTERNAL ONLY
BPAGE DRAWING
apl_ff.+V1P8.53
Fri May 27 06:47:26 2016
3nod三诺
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <WIFI/BT M.2 CONN>
Rev V01
Date: Saturday, March 25, 2017
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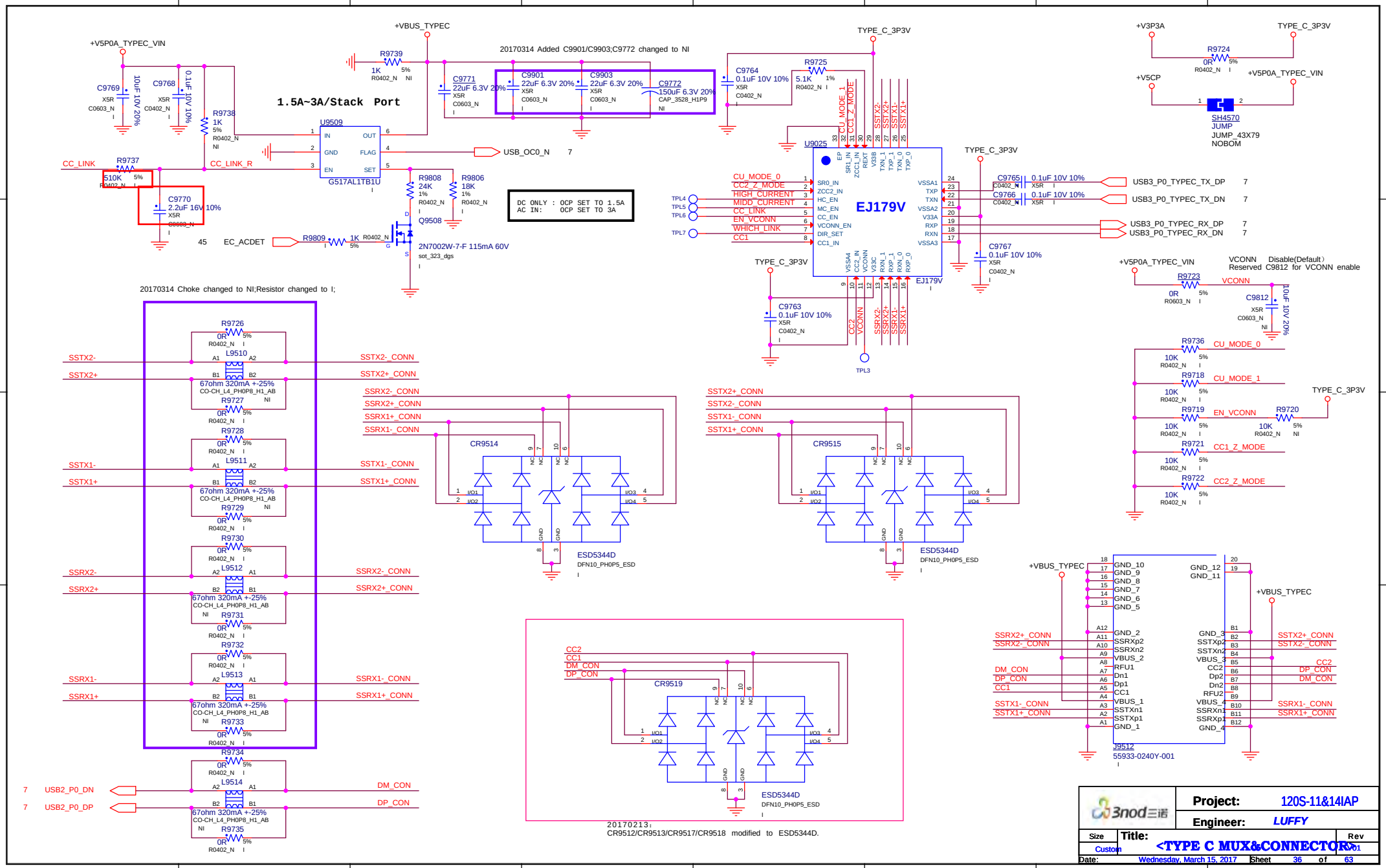

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HDMI LEVEL SHIFTER

+V1P8A — NOBOM — +V1P8A_HDMI
JUMP_43X39
SH9500
JUMP

6	DDI0_TX0_DP	DDI0_TX0_DP	C9580 0.1uF 10V 10% C0402_N X5R	HDMI_TX2_CMC_DP	
6	DDI0_TX0_DN	DDI0_TX0_DN	C9581 0.1uF 10V 10% C0402_N X5R	HDMI_TX2_CMC_DN	
6	DDI0_TX1_DP	DDI0_TX1_DP	C9582 0.1uF 10V 10% C0402_N X5R	HDMI_TX1_CMC_DP	
6	DDI0_TX1_DN	DDI0_TX1_DN	C9583 0.1uF 10V 10% C0402_N X5R	HDMI_TX1_CMC_DN	
6	DDI0_TX2_DP	DDI0_TX2_DP	C9584 0.1uF 10V 10% C0402_N X5R	HDMI_TX0_CMC_DP	
6	DDI0_TX2_DN	DDI0_TX2_DN	C9585 0.1uF 10V 10% C0402_N X5R	HDMI_TX0_CMC_DN	
6	DDI0_TX3_DP	DDI0_TX3_DP	C9586 0.1uF 10V 10% C0402_N X5R	HDMI_CLK_CMC_DP	
6	DDI0_TX3_DN	DDI0_TX3_DN	C9587 0.1uF 10V 10% C0402_N X5R	HDMI_CLK_CMC_DN	

R9528 0R 5% R0402_N NI
L4S12X20U 90ohm 100mA +-20%
HDMI_TX2_CMC_DP → HDMI_TX2_CONN_DP → HDMI_TX2_CONN_DP 38
HDMI_TX2_CMC_DN → HDMI_TX2_CONN_DN → HDMI_TX2_CONN_DN 38
L9508
R9529 0R 5% R0402_N

R9530 0R 5% R0402_N NI
L4S12X20U 90ohm 100mA +-20%
HDMI_TX1_CMC_DP → HDMI_TX1_CONN_DP → HDMI_TX1_CONN_DP 38
HDMI_TX1_CMC_DN → HDMI_TX1_CONN_DN → HDMI_TX1_CONN_DN 38
L9509
R9531 0R 5% R0402_N

R9532 0R 5% R0402_N NI
L4S12X20U 90ohm 100mA +-20%
HDMI_TX0_CMC_DP → HDMI_TX0_CONN_DP → HDMI_TX0_CONN_DP 38
HDMI_TX0_CMC_DN → HDMI_TX0_CONN_DN → HDMI_TX0_CONN_DN 38
L9506
R9533 0R 5% R0402_N

R9534 0R 5% R0402_N NI
L4S12X20U 90ohm 100mA +-20%
HDMI_CLK_CMC_DP → HDMI_CLK_CONN_DP → HDMI_CLK_CONN_DP 38
HDMI_CLK_CMC_DN → HDMI_CLK_CONN_DN → HDMI_CLK_CONN_DN 38
L9507
R9535 0R 5% R0402_N

+V5P0SX_HDMI — CR9500 BAT54A 200mA 30V SOT_23
VHDMI_SCL — R9577 2.2K R0402_N 5%
VHDMI_SDA — R9580 2.2K R0402_N 5%
38 HDMI_DDC_SCL — HDMI_DDC_SDA 38

+V1P8A_HDMI — Q9501 BSS138 300mA 50V sot23_gsd
+V1P8A_HDMI — Q9503 BSS138 300mA 50V sot23_gsd
R9579 2.2K R0402_N 5%
R9581 2.2K R0402_N 5%
6 DDI0_DDC_SCL — DDI0_DDC_SCL
6 DDI0_DDC_SDA — DDI0_DDC_SDA

HDMI_PLS_FET — Q9504 2N7002W-7-F 115mA 60V sot_323_dgs
40,45 EC_SLP_SX — R9682 100K 5% R0402_N

+V1P8A_HDMI — R9578 10K 5% R0402_N
DDI0_HPD_N — DDI0_HPD_N 6
Q9502 2N7002W-7-F 115mA 60V sot_323_dgs
HDMI_HPD — HDMI_HPD 38
R9576 100K 5% R0402_N

FET HAS BEEN CHANGED PLEASE REVIEW

HDMI_TX2_CMC_DP, HDMI_TX2_CMC_DN
HDMI_TX1_CMC_DP, HDMI_TX1_CMC_DN
HDMI_TX0_CMC_DP, HDMI_TX0_CMC_DN
HDMI_CLK_CMC_DP, HDMI_CLK_CMC_DN

20161228:
Changed from 680R to 470R

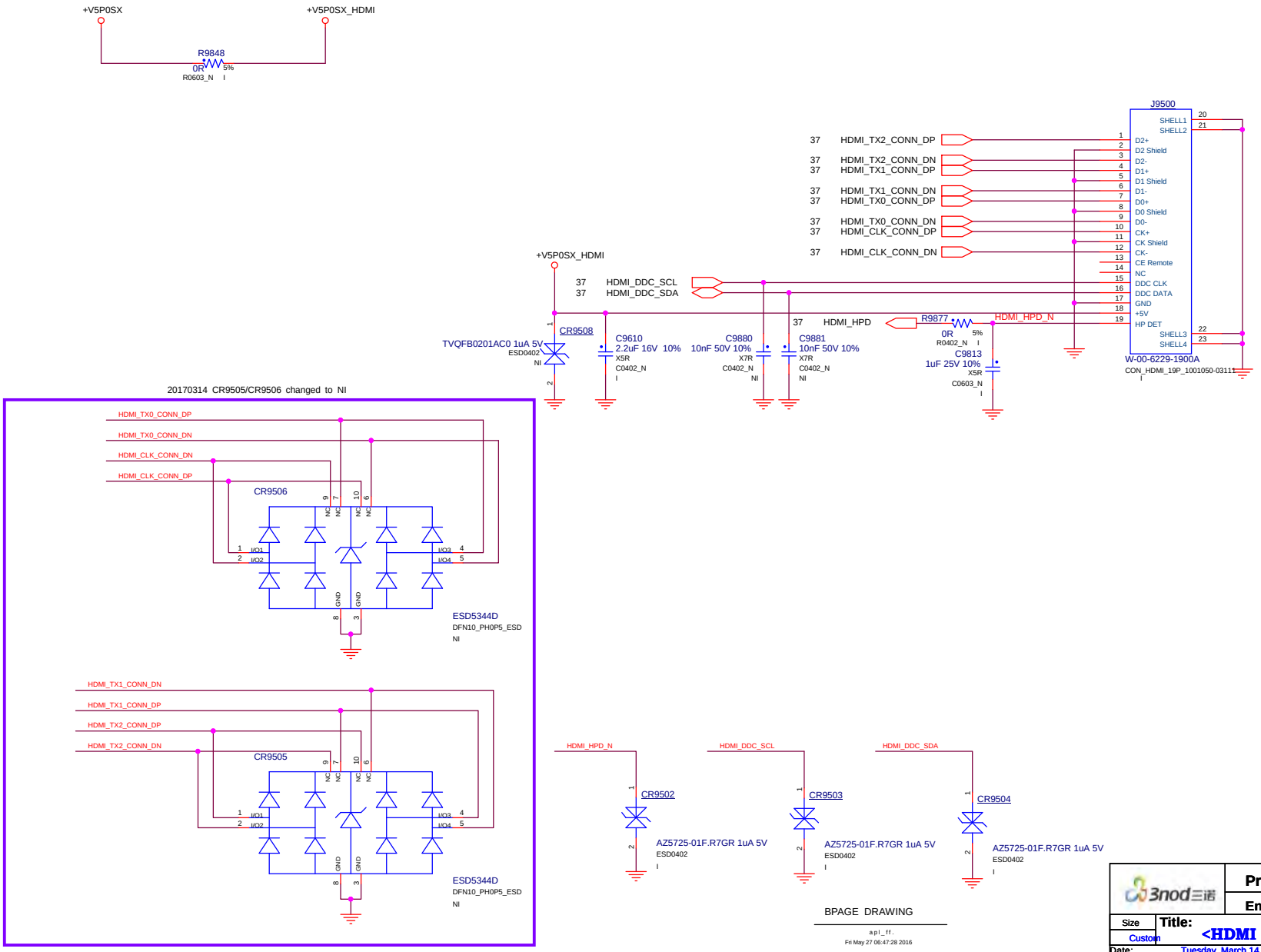
R9520 470R 1% R0402_N
R9521 470R 1% R0402_N
R9522 470R 1% R0402_N
R9523 470R 1% R0402_N
R9524 470R 1% R0402_N
R9525 470R 1% R0402_N
R9526 470R 1% R0402_N
R9527 470R 1% R0402_N

HDMI_PLS_FET

BPAGE DRAWING
apl_ll.8A
Fri May 27 06:47:26 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<HDMI LEVEL SHIFTER>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 37 of 63	

HDMI CONNECTOR



3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<HDMI CONN>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 38 of 63	

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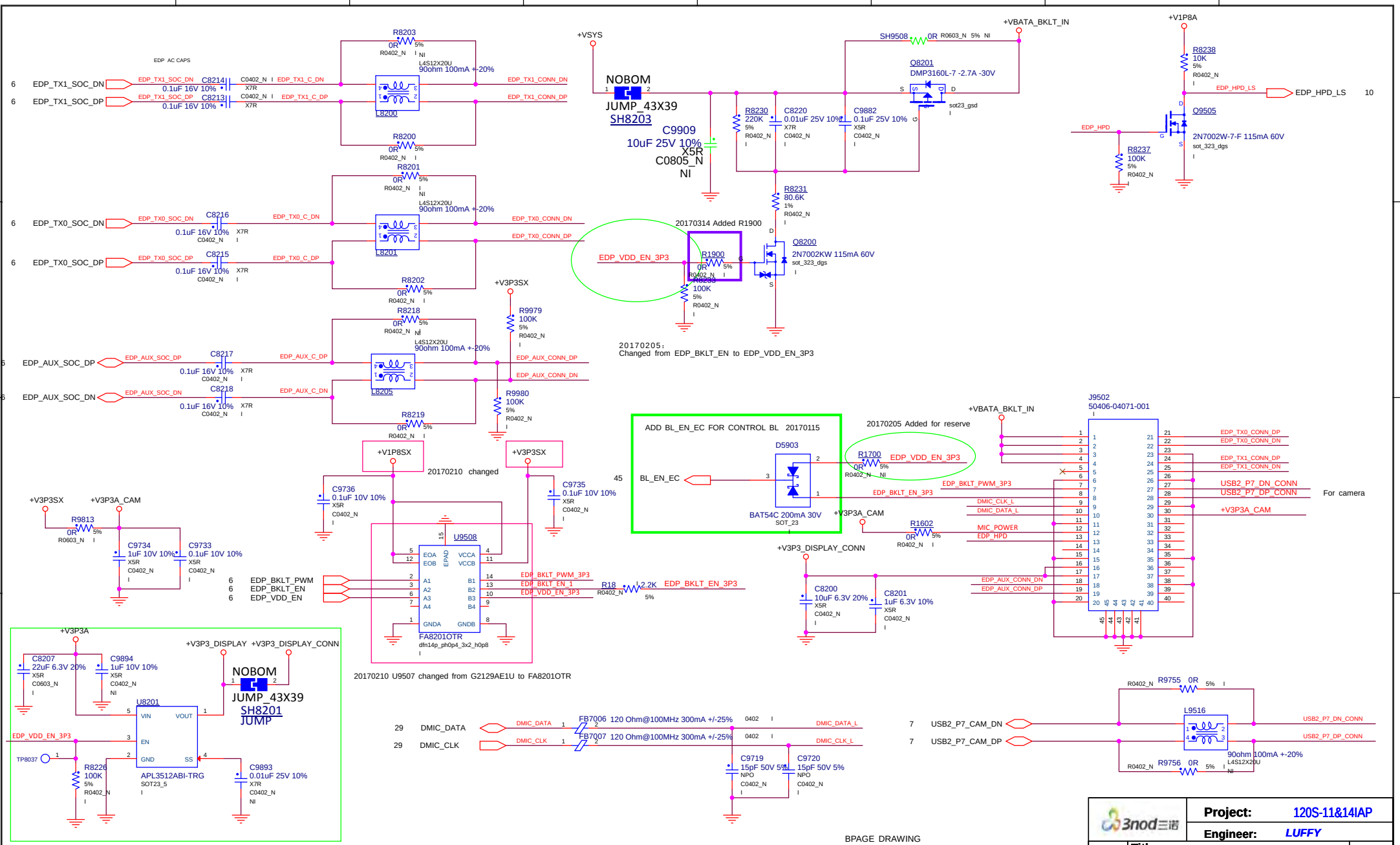
EDP_TX1_SOC_DN
EDP_TX1_SOC_DP
EDP_TX0_SOC_DN
EDP_TX0_SOC_DP
EDP_AUX_SOC_DP
EDP_AUX_SOC_DN
EDP_TX1_CONN_DN
EDP_TX1_CONN_DP
EDP_TX0_CONN_DN
EDP_TX0_CONN_DP
EDP_AUX_CONN_DP
EDP_AUX_CONN_DN
L8200
L8201
L8205
L4S12X20U
90ohm 100mA +-20%
+VSYS
NOBOM
JUMP_43X39
SH8203
C9909
10uF 25V 10%
X5R
C0805_N
NI
+VBATA_BKLT_IN
SH9508
Q8201
DMP3160L-7 -2.7A -30V
sot23_gsd
R8230
220K
C8220
0.01uF 25V 10%
C9882
0.1uF 25V 10%
R8231
80.6K
1%
R0402_N
20170314 Added R1900
EDP_VDD_EN_3P3
R1900
R8233
100K
Q8200
2N7002KW 115mA 60V
sot_323_dgs
20170205:
Changed from EDP_BKLT_EN to EDP_VDD_EN_3P3
+V1P8A
R8238
10K
EDP_HPD_LS
Q9505
2N7002W-7-F 115mA 60V
sot_323_dgs
EDP_HPD
R8237
100K
+V3P3SX
R9979
100K
R9980
100K
+V1P8SX
20170210 changed
C9736
0.1uF 10V 10%
C9735
0.1uF 10V 10%
+V3P3A_CAM
R9813
C9734
1uF 10V 10%
C9733
0.1uF 10V 10%
EDP_BKLT_PWM
EDP_BKLT_EN
EDP_VDD_EN
U9508
FA8201OTR
dfn14p_ph0p4_3x2_h0p8
EDP_BKLT_PWM_3P3
EDP_BKLT_EN_1
EDP_VDD_EN_3P3
R18
2.2K
EDP_BKLT_EN_3P3
20170210 U9507 changed from G2129AE1U to FA8201OTR
ADD BL_EN_EC FOR CONTROL BL 20170115
D5903
BAT54C 200mA 30V
SOT_23
BL_EN_EC
20170205 Added for reserve
R1700
+VBATA_BKLT_IN
J9502
50406-04071-001
EDP_BKLT_PWM_3P3
EDP_BKLT_EN_3P3
DMIC_CLK_L
DMIC_DATA_L
MIC_POWER
EDP_HPD
USB2_P7_DN_CONN
USB2_P7_DP_CONN
+V3P3A_CAM
For camera
R1602
+V3P3_DISPLAY_CONN
C8200
10uF 6.3V 20%
C8201
1uF 6.3V 10%
+V3P3A
C8207
22uF 6.3V 20%
C9894
1uF 10V 10%
+V3P3_DISPLAY
+V3P3_DISPLAY_CONN
NOBOM
JUMP_43X39
SH8201
JUMP
U8201
APL3512ABI-TRG
SOT23_5
EDP_VDD_EN_3P3
TP8037
R8226
100K
C9893
0.01uF 25V 10%
20170207 U8201 changed from WS4601E-5/TR to APL3512ABI-TRG
DMIC_DATA
DMIC_CLK
FB7006 120 Ohm@100MHz 300mA +/-25%
FB7007 120 Ohm@100MHz 300mA +/-25%
DMIC_DATA_L
DMIC_CLK_L
C9719
15pF 50V 5%
C9720
15pF 50V 5%
USB2_P7_CAM_DN
USB2_P7_CAM_DP
R9755
R9756
L9516
USB2_P7_DN_CONN
USB2_P7_DP_CONN
90ohm 100mA +-20%
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <DISPLAY>
Rev V01
Date: Tuesday, March 28, 2017
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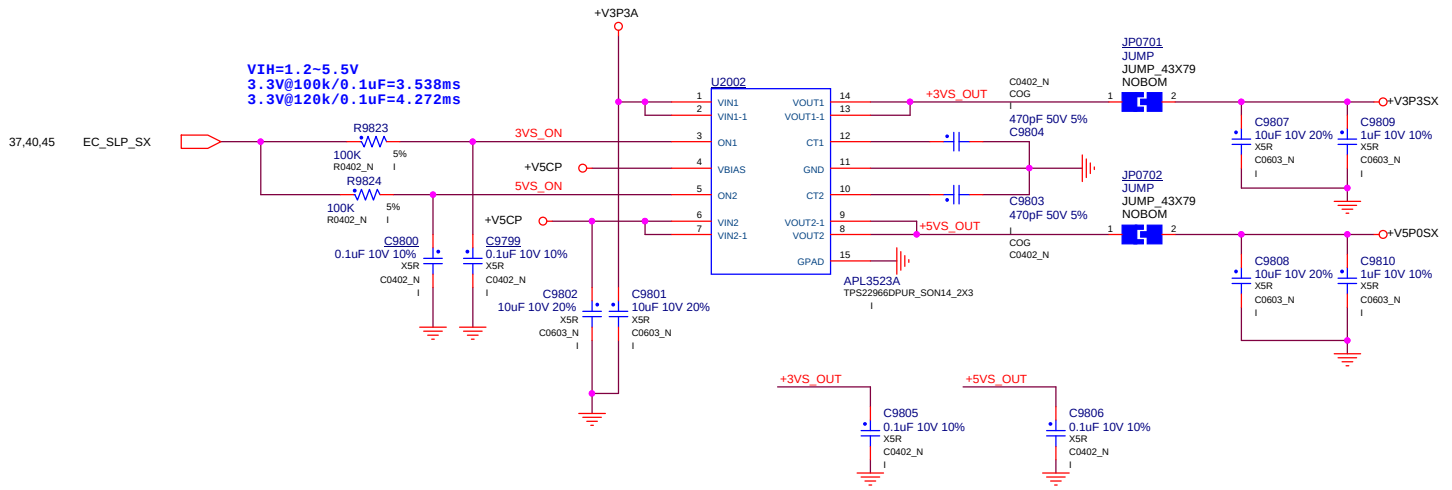

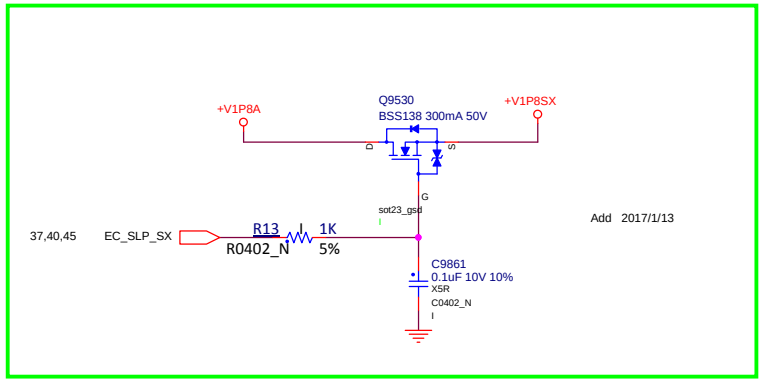

INTERNAL ONLY

BPAGE DRAWING

apl_lf.8A
Fri May 27 06:47:28 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: +V5P0A ,+V3P3SX,+V5P0SX	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 40 of 63	

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[PAGE_TITLE= TI PMIC 1 OF 4]

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:28 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
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BPAGE DRAWING

apl_ff.UNS13.137
Fri May 27 06:47:30 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	*LUFFY*
Size: Custom	Title: <NC>	Rev: V01
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BPAGE DRAWING

apl_ll.8A
Fri May 27 06:47:30 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: *LUFFY*	
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 43 of 63	

[PAGE_TITLE=TI PMIC 4 OF 4]

BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:30 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 44 of 63	

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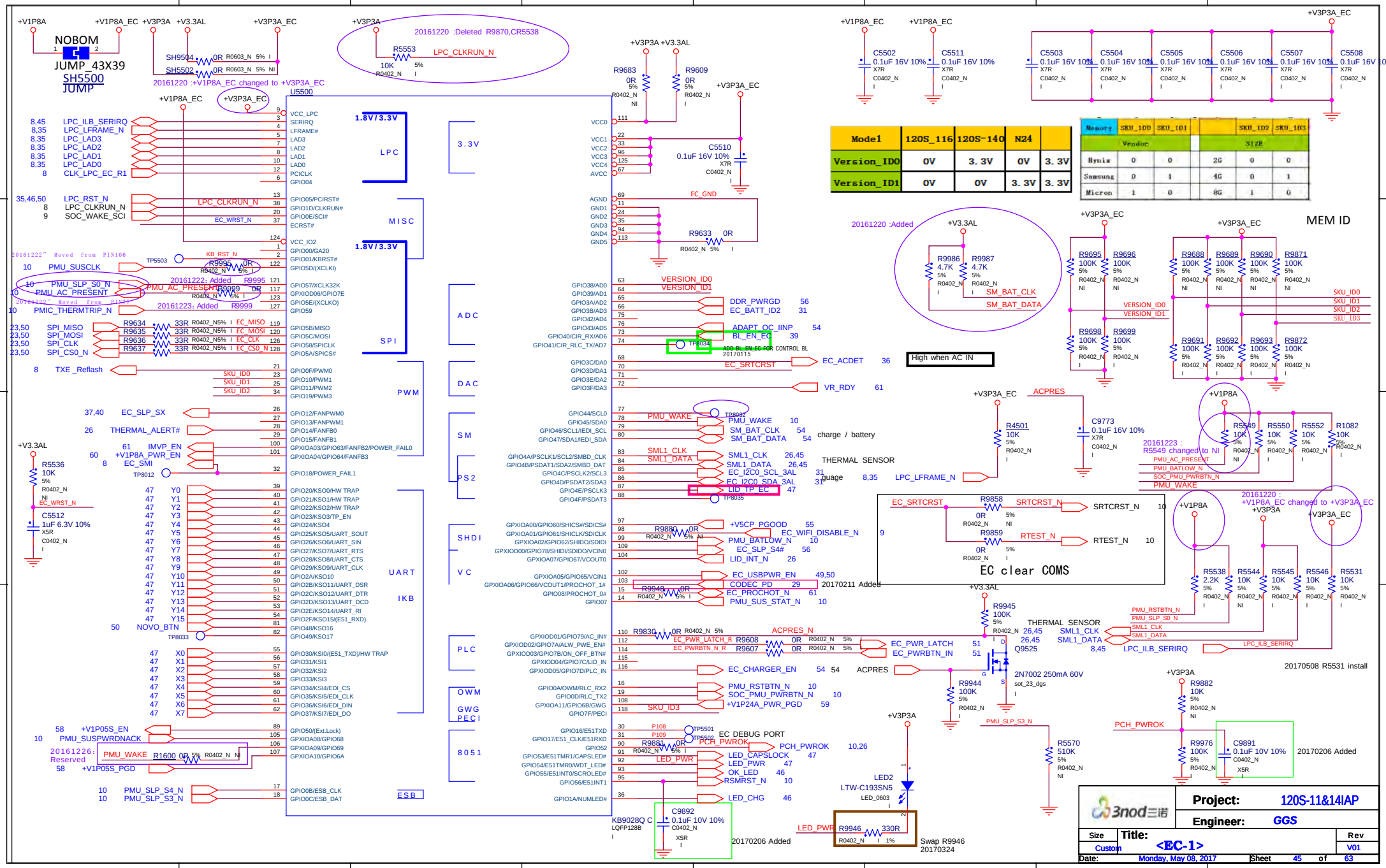
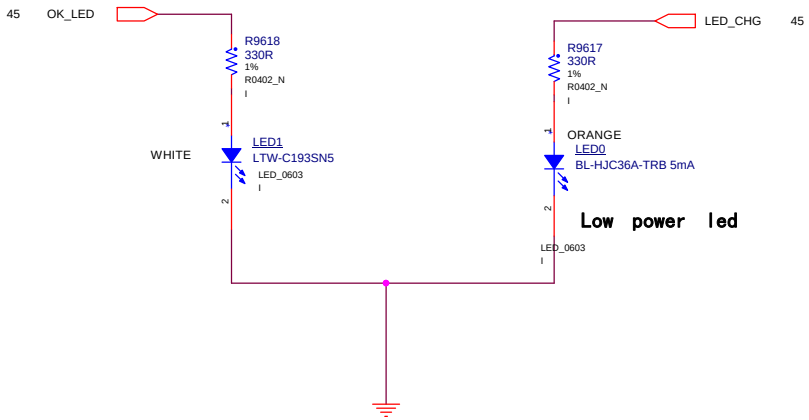
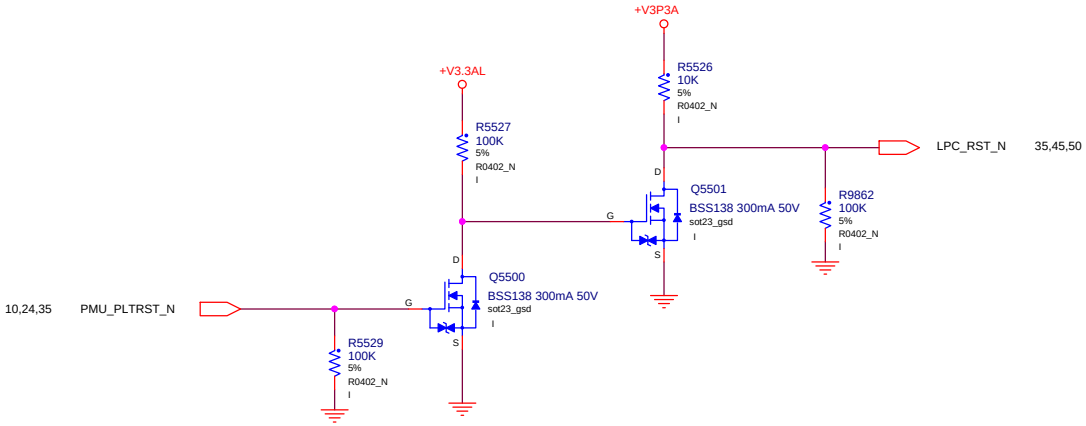


Mode1	120S_116	120S-140	N24	
Version_ID0	0V	3.3V	0V	3.3V
Version_ID1	0V	0V	3.3V	3.3V

Memory	SKU_ID0	SKU_ID1		SKU_ID2	SKU_ID3
Vendor			SIZE		
Hynix	0	0	2G	0	0
Samsung	0	1	4G	0	1
Micron	1	0	8G	1	0

MEM ID





NOTE: CHECK RESET CONNECTION

BPAGE DRAWING

apl_tf.UN$14.141
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: LED AND BUTTON	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 46 of 63	

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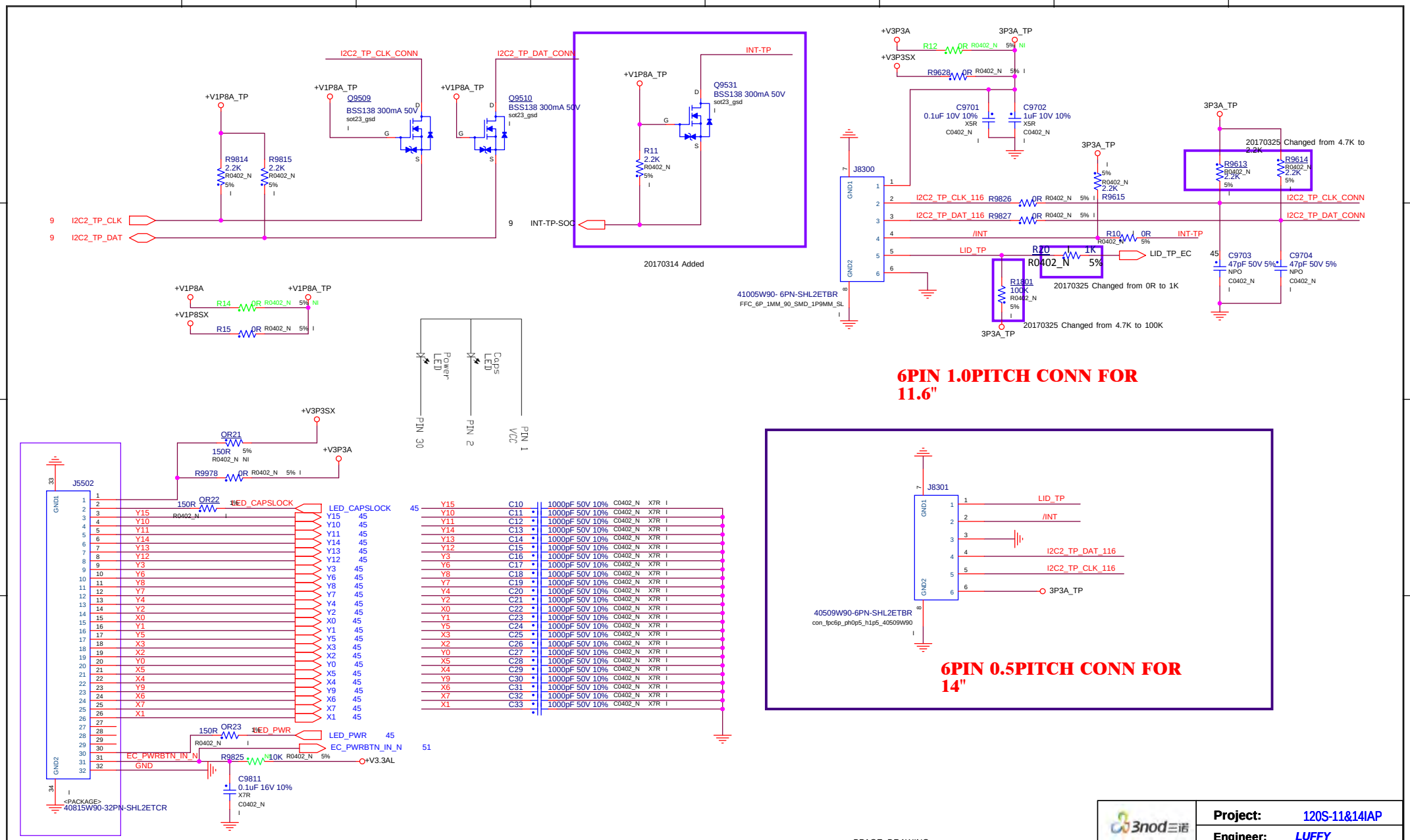
I2C2_TP_CLK_CONN
I2C2_TP_DAT_CONN
INT-TP
+V1P8A_TP
Q9509
BSS138 300mA 50V
Q9510
BSS138 300mA 50V
Q9531
BSS138 300mA 50V
R9814 2.2K
R9815 2.2K
R11 2.2K
I2C2_TP_CLK
I2C2_TP_DAT
INT-TP-SOC
20170314 Added
+V3P3A
+V3P3SX
3P3A_TP
R12 0R
R9628 0R
C9701 0.1uF 10V 10%
C9702 1uF 10V 10%
J8300
I2C2_TP_CLK_116
I2C2_TP_DAT_116
R9826 0R
R9827 0R
R9613 2.2K
R9614 2.2K
20170325 Changed from 4.7K to 2.2K
R9615 2.2K
/INT
LID_TP
R10 0R
R20 1K
LID_TP_EC
R1801 100K
20170325 Changed from 0R to 1K
20170325 Changed from 4.7K to 100K
C9703 47pF 50V 5%
C9704 47pF 50V 5%
41005W90- 6PN-SHL2ETBR
FFC_6P_1MM_90_SMD_1P9MM_SL
6PIN 1.0PITCH CONN FOR 11.6"
+V1P8A
+V1P8SX
R14 0R
R15 0R
Power LED
Caps LED
PIN 30
PIN 2
PIN 1
VCC
+V3P3SX
+V3P3A
OR21 150R
R9978 0R
J5502
LED_CAPSLOCK
LED_PWR
EC_PWRBTN_IN_N
GND
OR22 150R
OR23 150R
R9825 10K
+V3.3AL
C9811 0.1uF 16V 10%
40815W90-32PN-SHL2ETCR
20161226:
J5502 PIN SWAP
J8301
LID_TP
/INT
I2C2_TP_DAT_116
I2C2_TP_CLK_116
3P3A_TP
40509W90-6PN-SHL2ETBR
con_fpc6p_ph0p5_h1p5_40509W90
6PIN 0.5PITCH CONN FOR 14"
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: KEY BOARD,TP
Rev: V01
Date: Monday, May 08, 2017
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BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	*LUFFY*
Size: Custom	Title: <NC>	Rev: V01
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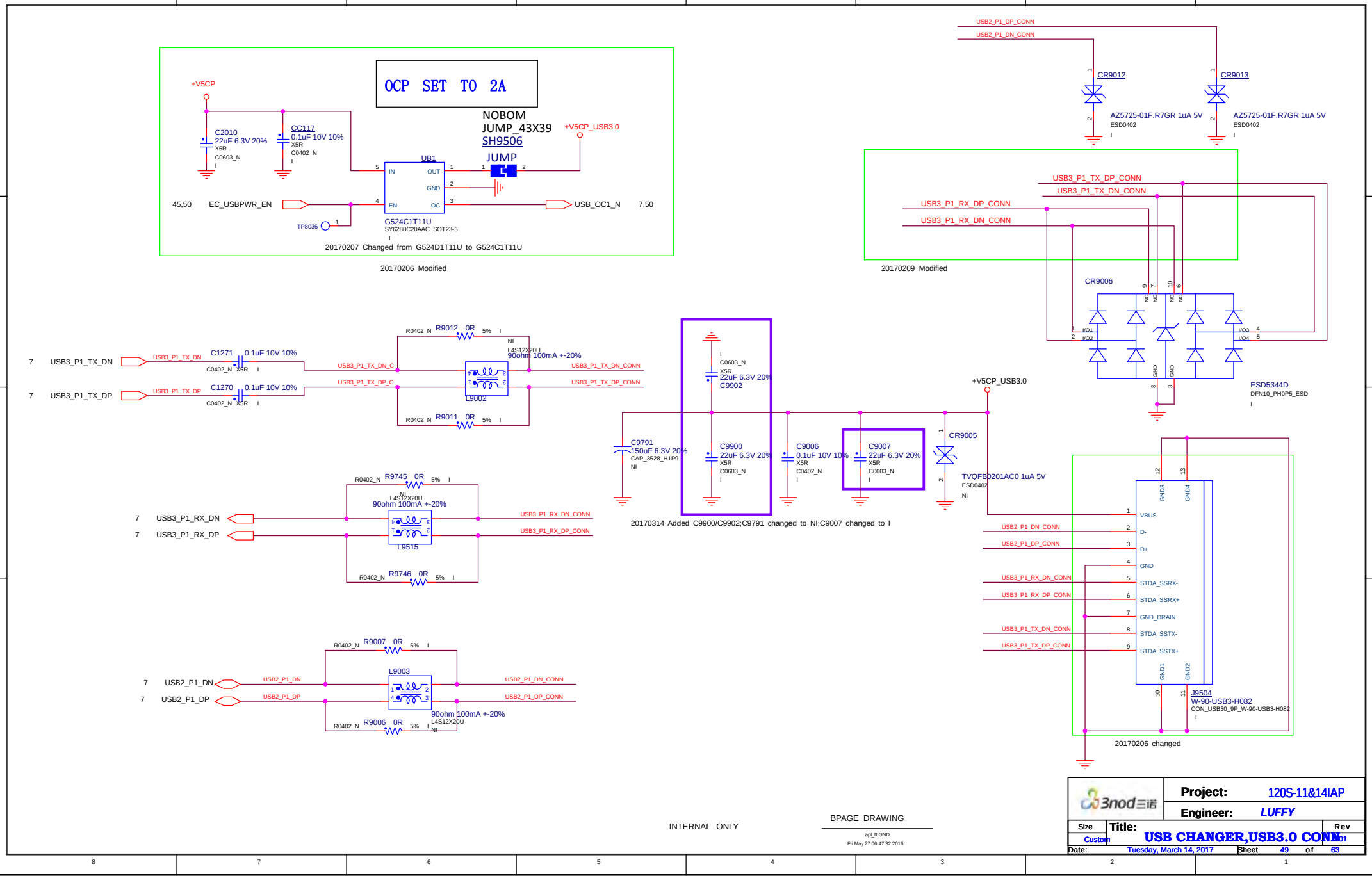
OCP SET TO 2A
NOBOM
JUMP_43X39
SH9506
JUMP
+V5CP
+V5CP_USB3.0
C2010
22uF 6.3V 20%
X5R
C0603_N
CC117
0.1uF 10V 10%
X5R
C0402_N
UB1
IN
OUT
GND
EN
OC
45,50
EC_USBPWR_EN
USB_OC1_N
7,50
TP8036
G524C1T11U
SY6288C20AAC_SOT23-5
20170207 Changed from G524D1T11U to G524C1T11U
20170206 Modified
USB2_P1_DP_CONN
USB2_P1_DN_CONN
CR9012
CR9013
AZ5725-01F.R7GR 1uA 5V
ESD0402
USB3_P1_TX_DP_CONN
USB3_P1_TX_DN_CONN
USB3_P1_RX_DP_CONN
USB3_P1_RX_DN_CONN
20170209 Modified
CR9006
ESD5344D
DFN10_PH0P5_ESD
R0402_N
R9012
0R
5%
NI
L4S12X20U
90ohm 100mA +-20%
7
USB3_P1_TX_DN
USB3_P1_TX_DP
C1271
C1270
0.1uF 10V 10%
C0402_N
X5R
USB3_P1_TX_DN_C
USB3_P1_TX_DP_C
USB3_P1_TX_DN_CONN
USB3_P1_TX_DP_CONN
L9002
R9011
C0603_N
C9902
22uF 6.3V 20%
C9791
150uF 6.3V 20%
CAP_3528_H1P9
C9900
22uF 6.3V 20%
C9006
0.1uF 10V 10%
C9007
22uF 6.3V 20%
CR9005
TVQFB0201AC0 1uA 5V
ESD0402
20170314 Added C9900/C9902;C9791 changed to NI;C9007 changed to I
R9745
R9746
USB3_P1_RX_DN
USB3_P1_RX_DP
USB3_P1_RX_DN_CONN
USB3_P1_RX_DP_CONN
L9515
R9007
R9006
USB2_P1_DN
USB2_P1_DP
USB2_P1_DN_CONN
USB2_P1_DP_CONN
L9003
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
GND1
GND2
GND3
GND4
J9504
W-90-USB3-H082
CON_USB30_9P_W-90-USB3-H082
20170206 changed
INTERNAL ONLY
BPAGE DRAWING
apl_ff.GND
Fri May 27 06:47:32 2016
Project: 120S-11&14IAP
Engineer: LUFFY
Size
Custom
Title: USB CHANGER,USB3.0 CONN
Rev
Date: Tuesday, March 14, 2017
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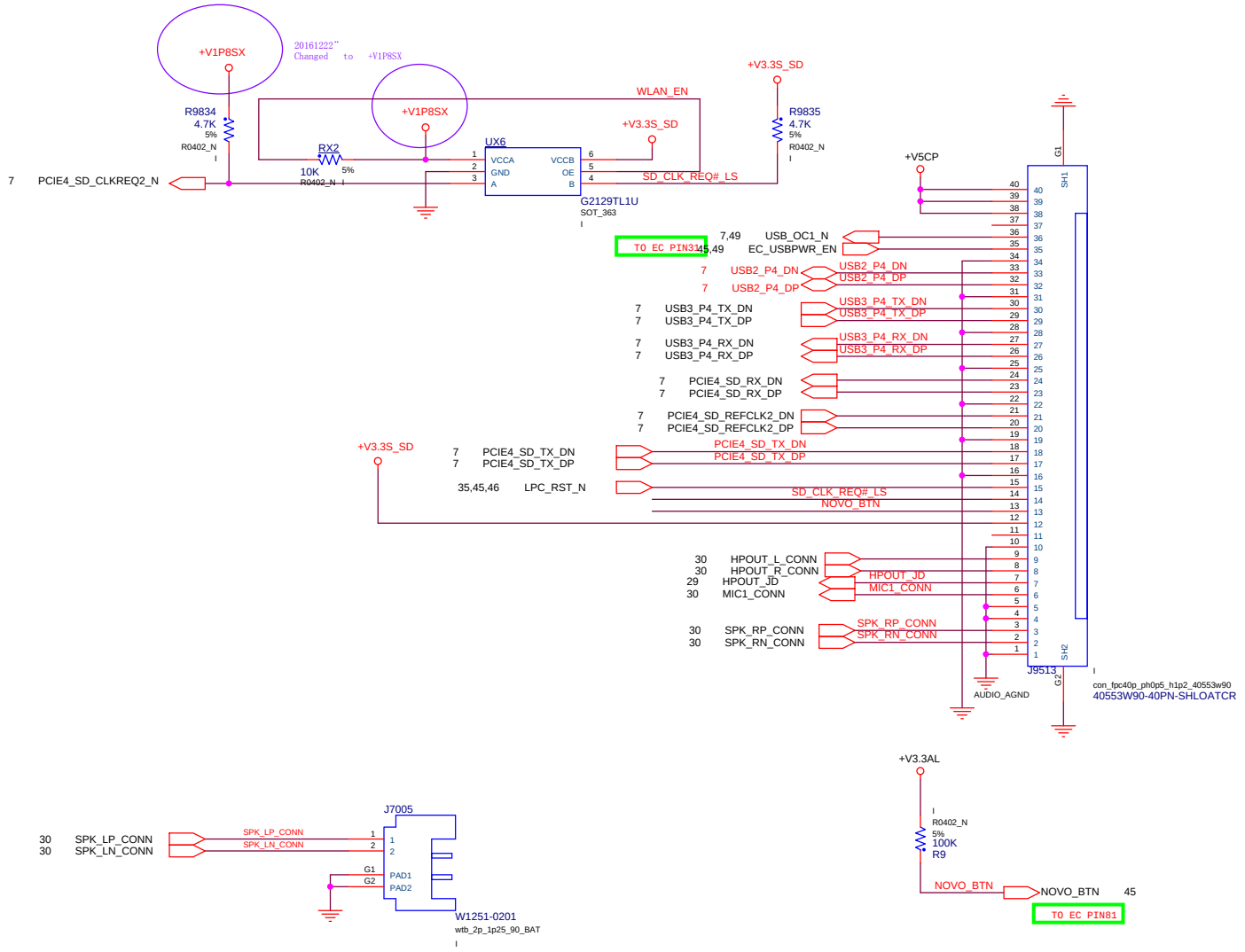
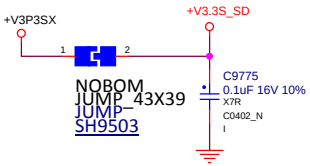
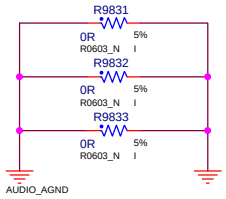
SD CARD POWER SUPPLY







BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<IO&DEBUG CONN>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 50 of 63	

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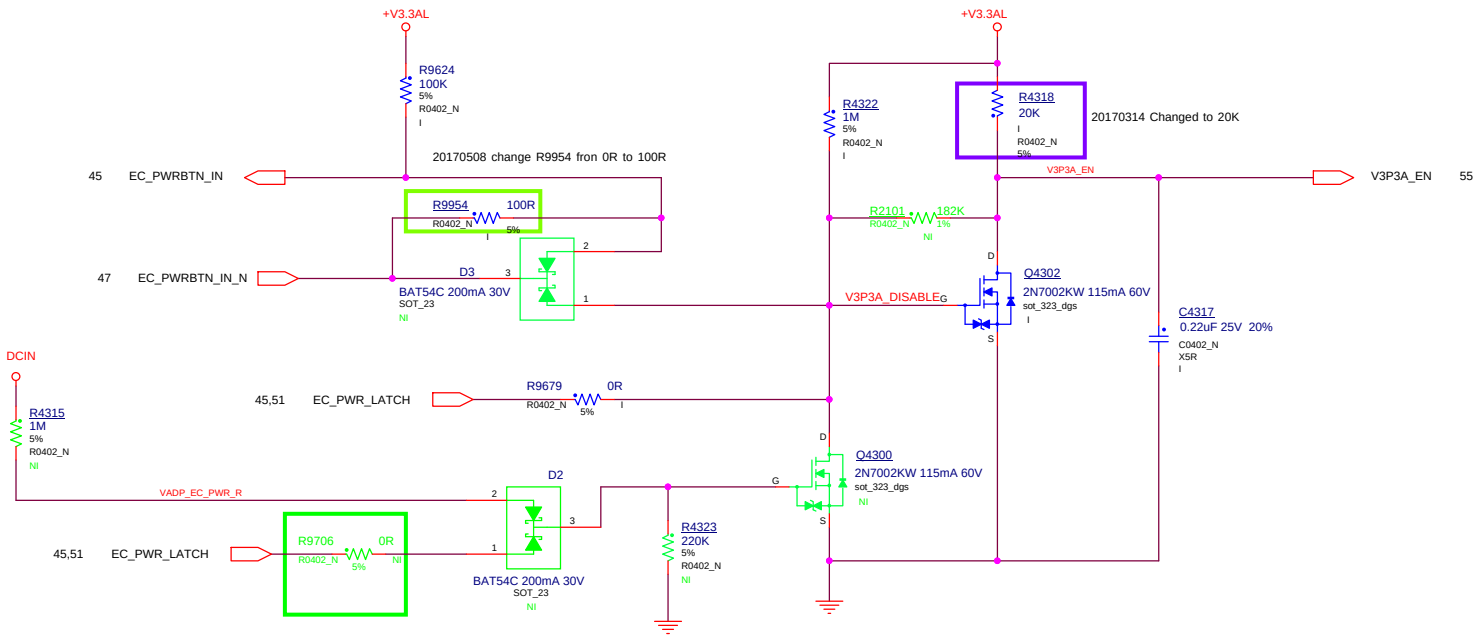

CHANGE TO NI 20170115

BPAGE DRAWING

apl_ff.UN$20.203
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <MISC>	Rev: V01
Date: Monday, May 08, 2017	Sheet 51 of 63	

INTERNAL ONLY

BPAGE DRAWING

apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 52 of 63	

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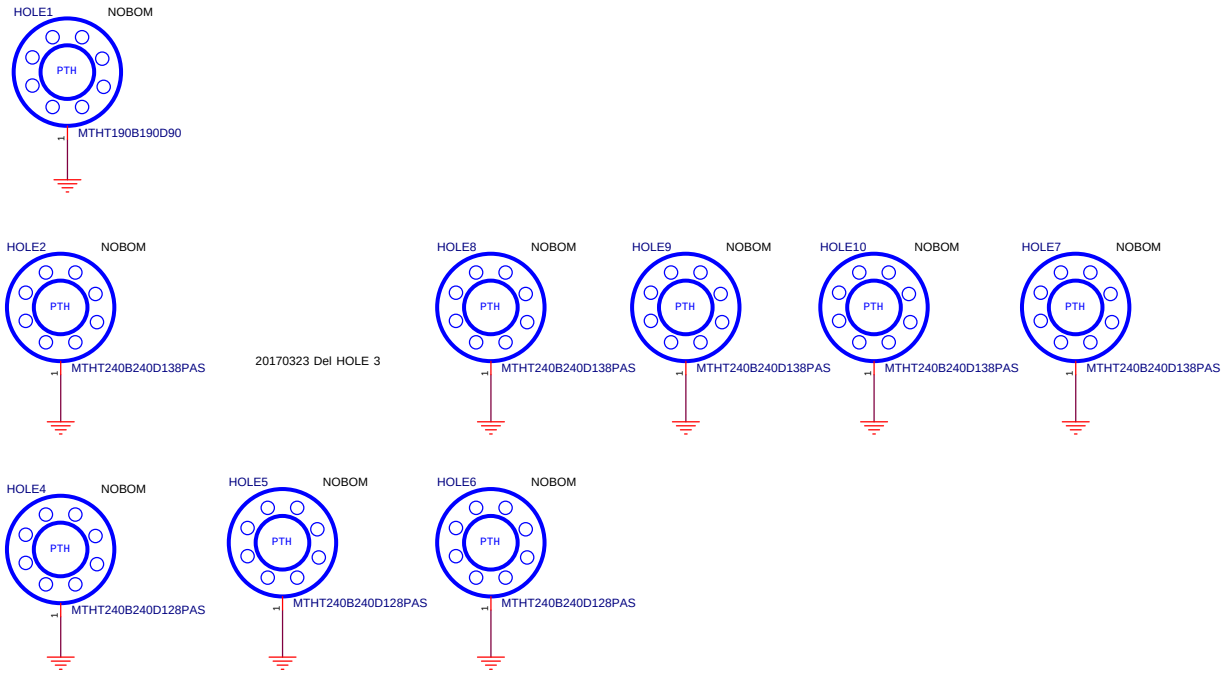


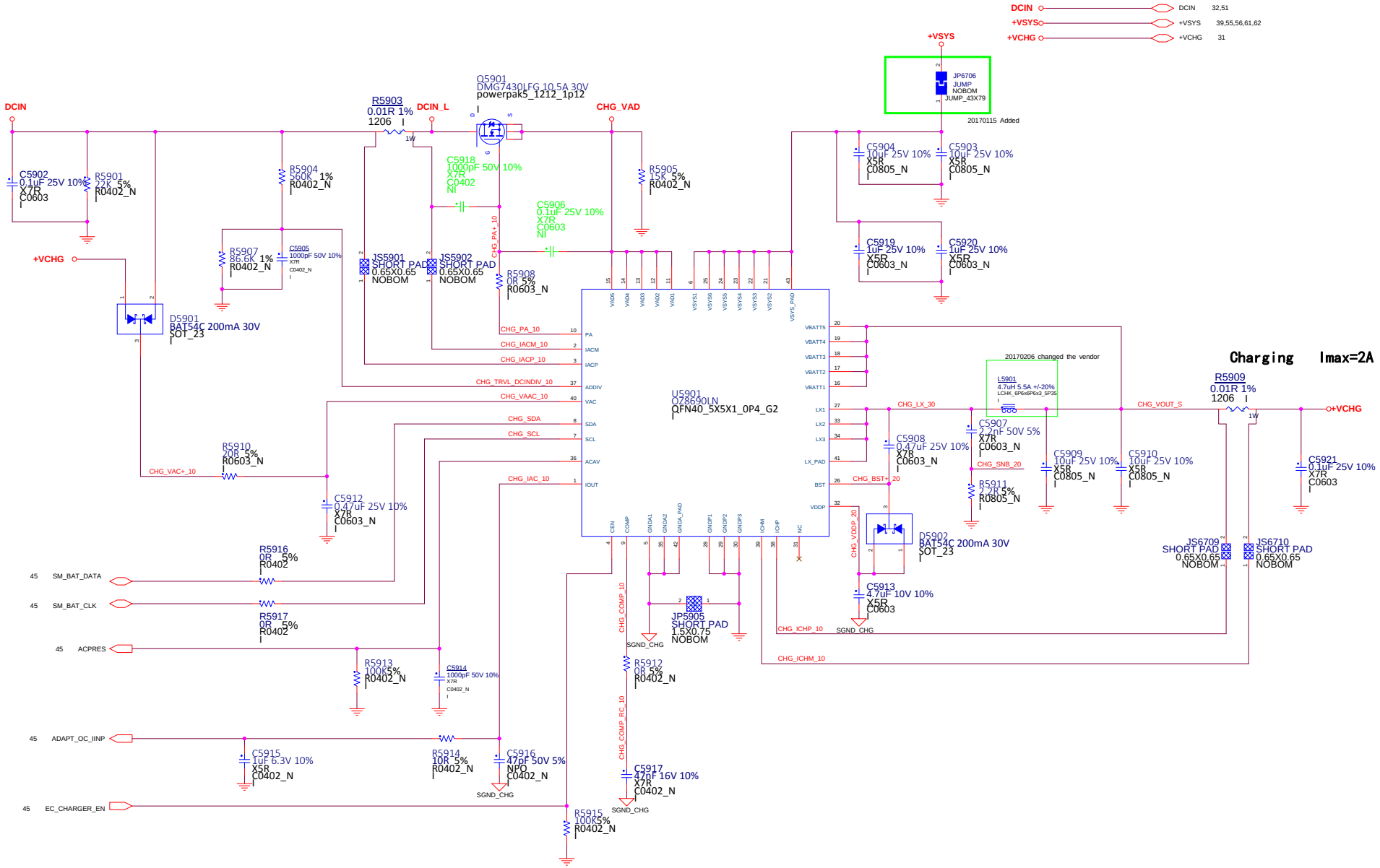
INTERNAL ONLY

BPAGE DRAWING

apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <SCREW>	Rev: V01
Date: Friday, March 24, 2017	Sheet 53 of 63	

59: BATTERY CHARGER



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size: Custom	Title: <BatteryCharger>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 54 of 63	

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+VSYS
SH2000 JUMP JUMP_43X79 NOBOM
+VSYS_V3P0AVR_IN

20170214 Deleted C9877,C2005

C2028 0.1uF 25V 10% X5R C0402_N
C2000 10uF 25V 10% X5R C0805_N
C2002 10uF 25V 10% X5R C0805_N
C2008 10uF 25V 10% X5R C0805_N

U2000

26 +V3P3A_SHUTDOWN# — R9994 0R 5% R0402_N — V3P3A_EN
51 V3P3A_EN

20161220 :Added

+V3.3AL — R9702 20K 5% R0402_N
20170214 Changed to182K
20170314 Changed to 20K

C2006 4.7uF 6.3V 20% X5R C0402_N

+V3.3AL — R2012 20K 5% R0402_N — V3P3A_PGOOD
20170314 Changed to 20K

C9889 1uF 6.3V 10% X5R C0402_N
C2011 1uF 6.3V 10% X5R C0402_N
AGND_3P3AVR
20170206 Added

+VCC3P6_VRA

VIN, CLK, EN, LDO, ENCLK, BST, SW, VOUT, PGND, AGND, PG, VCC

NB680GD QFN12_PH0P5_2X3_H1

SH2002 ETCH EMPTY
AGND_3P3AVR

V3P3A_BST — R2028 2.2R 1% R0402_N — V3P3A_BST_R — C2012 0.22uF 25V 20% X5R C0402_N

V3P3A_LX — L2001 1.5uH 10A 20% SML6673_H3

V3P3A_OUT
C2059 22uF 6.3V 20% X5R C0603_N
C2060 22uF 6.3V 20% X5R C0603_N
C2061 22uF 6.3V 20% X5R C0603_N
C2062 22uF 6.3V 20% X5R C0603_N
C2021 0.1uF 16V 10% X7R C0402_N

20170214 Deleted C2066、C2071 ;
C2021 changed to I;

+V3P3A
SH2004 JUMP JUMP_43X79 NOBOM

Imax=8A

+VSYS_V5P0AVR_IN
+VSYS
SH2001 JUMP JUMP_43X79 NOBOM

C2064 0.1uF 25V 10% X5R C0402_N
C2001 10uF 25V 10% X5R C0805_N
C2003 10uF 25V 10% X5R C0805_N
C2007 10uF 25V 10% X5R C0805_N NI
C2009 10uF 25V 10% X5R C0805_N

U2001

R9952 20K 5% R0402_N — V3P3A_PGOOD
20170207 Deleted R9951;R9952 changed to 100K;
EN control changed to V3P3A_PGOOD;
20170314 R9952 changed to 20K

+5VAL — C9797 0.1uF 16V X7R C0402_N

VIN, NC, EN, LDO, ENLDO, BST, SW, VOUT, PGND, AGND, PG, VCC

NB679GD QFN12_PH0P5_2X3_H1

SH2003 ETCH EMPTY
AGND_5P0AVR

45 +V5CP_PGOOD — +V5CP_PGOOD

+VCC3P6_VRB
C9890 1uF 6.3V 10% X5R C0402_N
C2073 1uF 6.3V 10% X5R C0402_N
AGND_5P0AVR
20170206 Added

+V3.3AL — R2000 100K 5% R0402_N

VCC_V5CP_BST — R2029 2.2R 1% R0402_N — VCC_V5CP_BST_R — C2013 0.22uF 25V 20% X5R C0402_N

+V5CP_LX — L2000 1.5uH 10A 20% SML6673_H3

+V5CP_OUT
C9866 22uF 6.3V 20% X5R C0603_N
C9867 22uF 6.3V 20% X5R C0603_N
C9868 22uF 6.3V 20% X5R C0603_N
C9869 22uF 6.3V 20% X5R C0603_N
C9870 22uF 6.3V 20% X5R C0603_N
C9871 22uF 6.3V 20% X5R C0603_N

+V5CP_OUT
C9904 22uF 6.3V 20% X5R C0603_N NI
C9905 22uF 6.3V 20% X5R C0603_N NI
C2056 0.1uF 16V 10% X7R C0402_N

20170316 Deleted C9899,Reserved C9904/C9905;

SH2007 JUMP JUMP_43X79 NOBOM
+V5CP

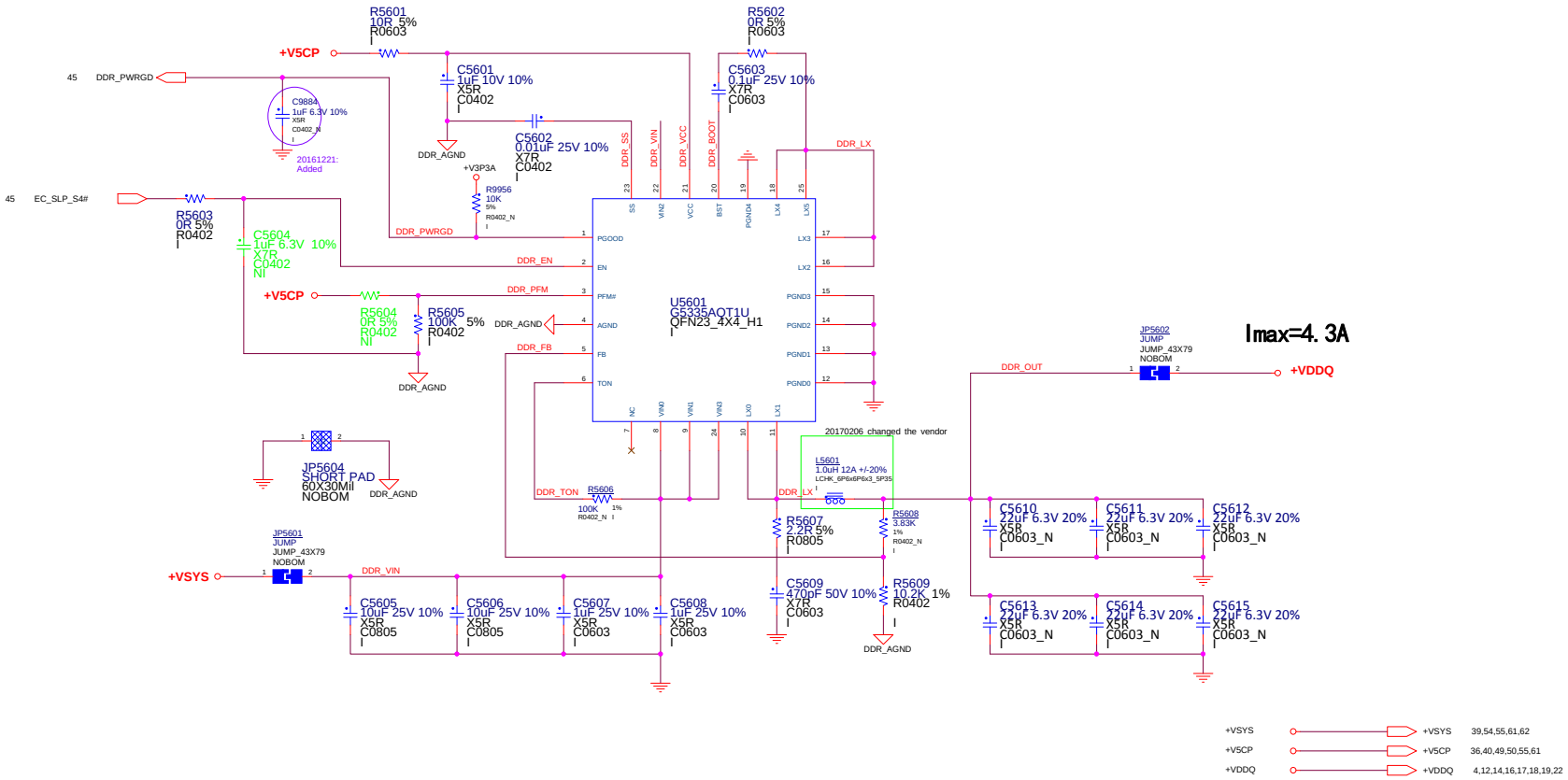
Imax=8A

INTERNAL ONLY

BPAGE DRAWING
apl_lf.8A
Fri May 27 06:47:28 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <PWR +V3P3A AND +5CP>	Rev: V01
Date: Thursday, March 16, 2017	Sheet 55 of 63	

56: DDR POWER SUPPLY



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <DDR Power>	Rev V01
Date: Tuesday, March 14, 2017	Sheet 56 of 63	

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3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <NC>	Rev V01
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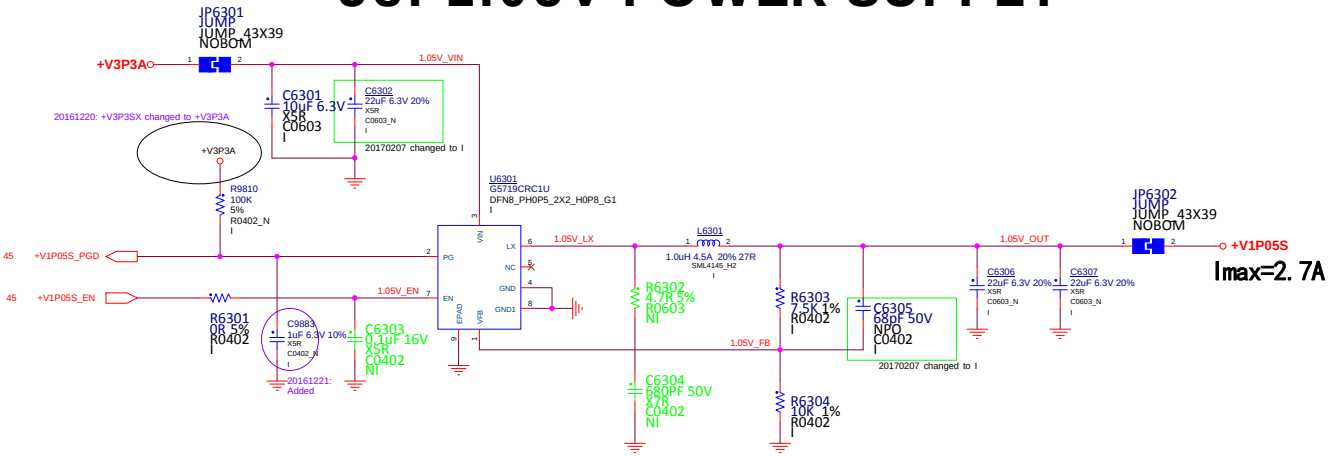
58: 1.05V POWER SUPPLY



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <1.05V POWER SUPPLY>	Rev V01
Date: Tuesday, March 14, 2017	Sheet 58 of 63	

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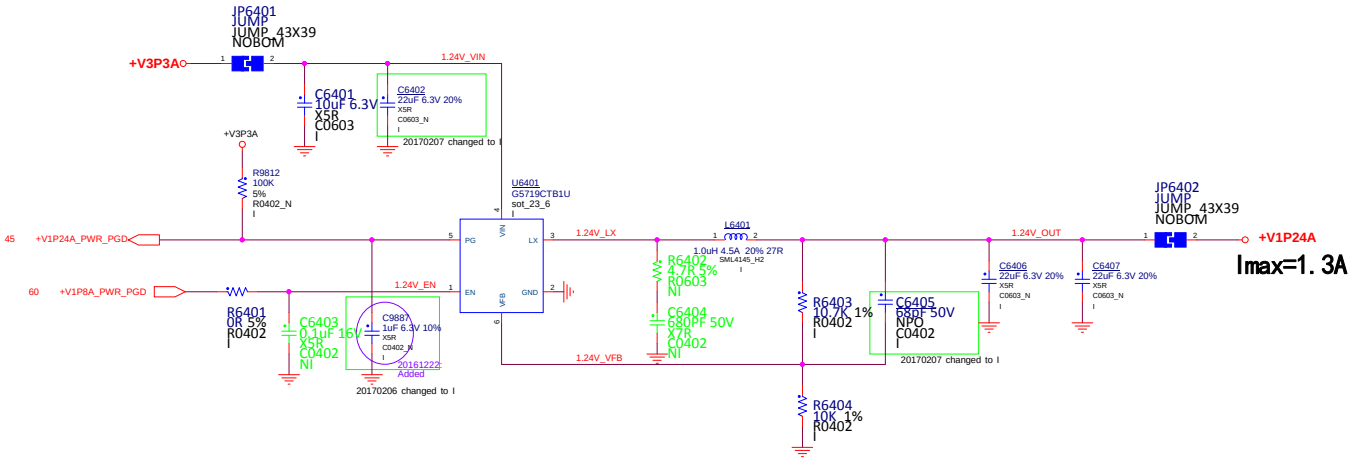
59: 1.24V POWER SUPPLY



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <1.24V POWER SUPPLY>	Rev V01
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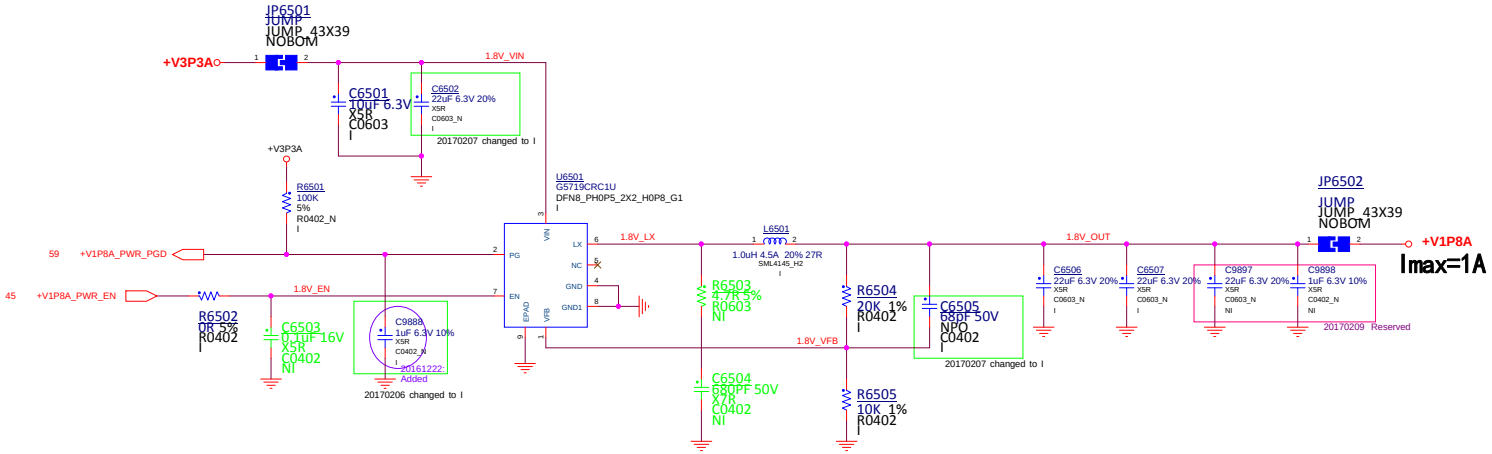
60: +1.8V POWER SUPPLY



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <+1.8V_PRIM>	Rev V01
Date: Tuesday, March 14, 2017	Sheet 60 of 63	

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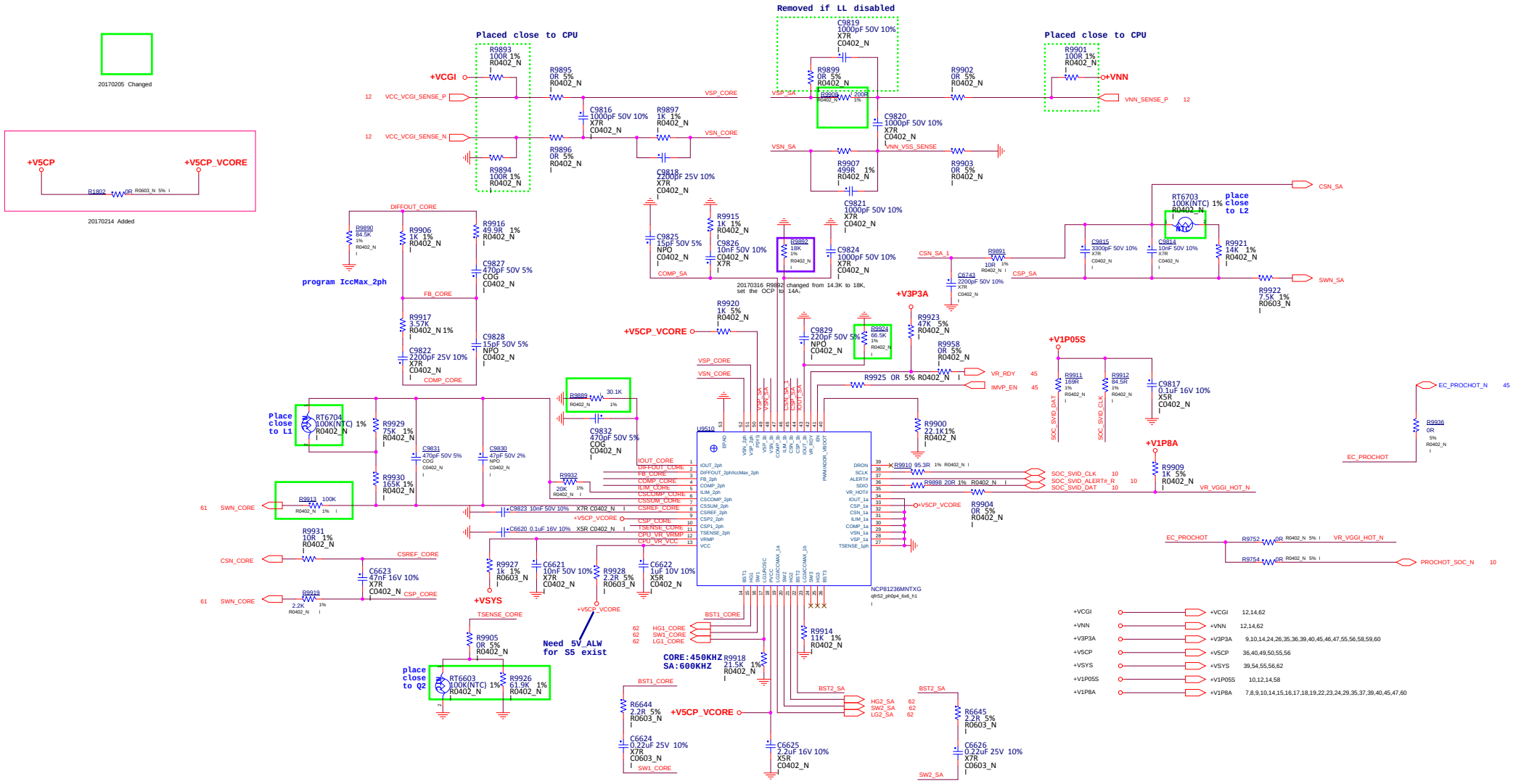
CPU POWER SUPPLY



3nod三诺	Project: NA	
	Engineer: Frank	
Size	Title: <VCGI AND VNN_1>	Rev
Custom		V01
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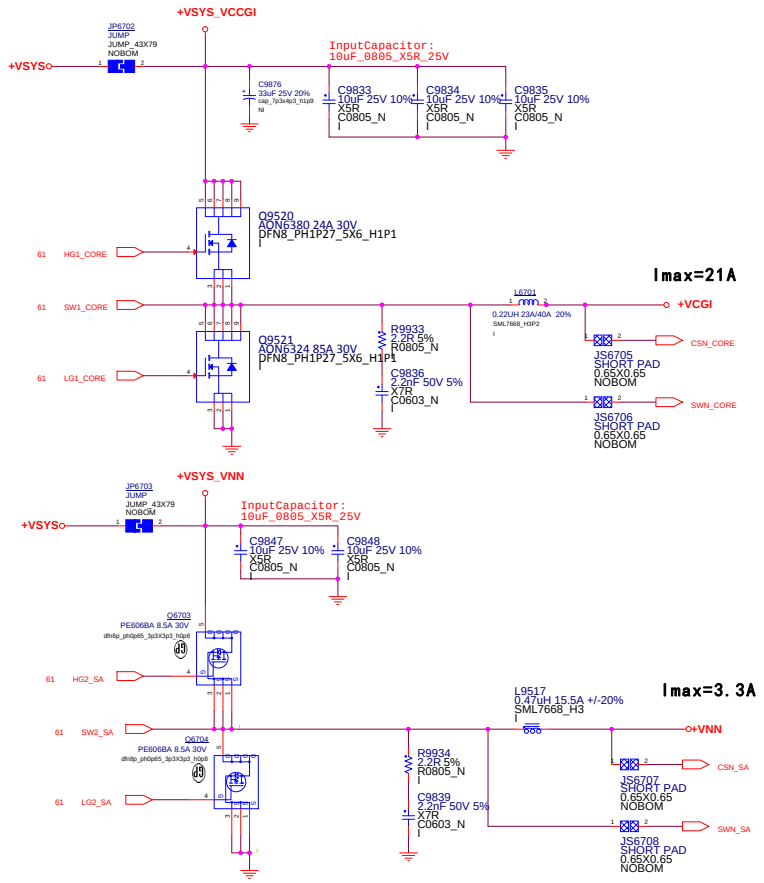
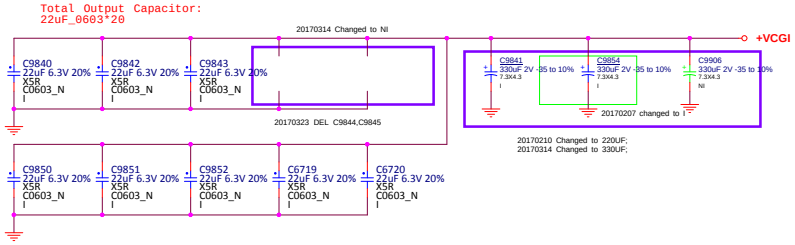
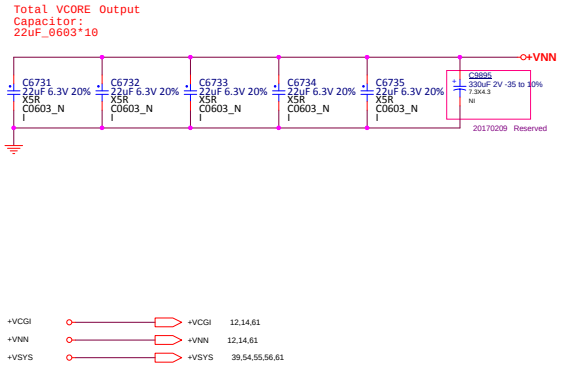
VCGI / VNN POWER SUPPLY







3nod三诺	Project: NA	
	Engineer: Frank	
Size: Custom	Title: <VCGI AND VNN_2>	Rev: V01
Date: Thursday, March 23, 2017	Sheet 62 of 63	

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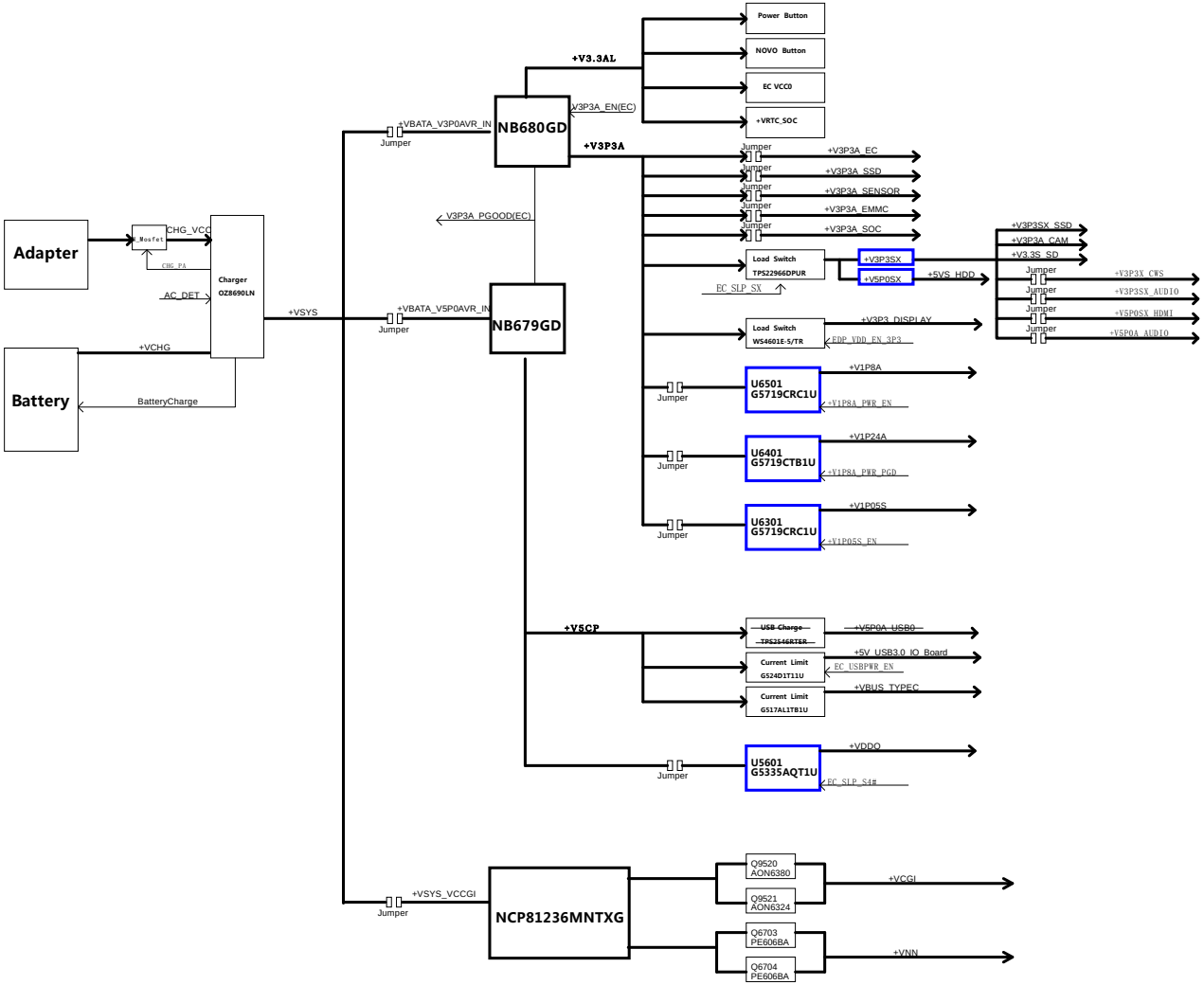
Apollo Lake Platform Power Map



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <PWR BLOCK DIAGRAM>	Rev V01
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